A boundary scan linker mux (multiplexer) device, also known as JTAG scan bridge or scan path linker, is a device that will be able to link or join multiple boundary scan chains into one single chain or multiple chain configurations depending on how the boundary scan linker mux device is configured. See Figure 1 below for a typical boundary scan linker mux connection.

The Lattice BSCAN2 allows multiple boundary scan chains or devices to be chained or isolated at the same time, by configuring access in accordance with the device family or as desired by the designer.

Figure 1. The boundary scan linker mux device BSCAN2 joins chain 1 (FPGA, CPLD, ASIC), chain 2 (ASIC, FPGA) and chain 3 (uP, ASIC, DSP)
Adding Ports by Chaining BSCAN2 ‘Top_Link’ Module

The ‘top_link’ BSCAN2 IP modules can be programmed into supported Lattice FPGA/CPLD as multiple BSCAN2 macros and can be chained together to increase the number of available BSCAN2 ports. This is accomplished by connecting TDO of one BSCAN2 to TDI of another BSCAN2, as shown in Figure 2.

Note: Figure 2 is from lattice application note AN8081 (Using Multiple Boundary Scan Port Linker (BSCAN2)).

![Figure 2: Adding ports by chaining BSCAN2 top_linker modules](image)

Implementation of Lattice BSCAN2 into Keysight x1149 Boundary Scan Analyzer

The Lattice BSCAN2 can be configured using Keysight x1149 ISL (Insert Source Language) using both the JTAG Technologies model or the ASSET Model.

**BSCAN2 registers**

<table>
<thead>
<tr>
<th>Register name</th>
<th>Type</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction</td>
<td>IR</td>
<td>8</td>
</tr>
<tr>
<td>Select</td>
<td>DR</td>
<td>8</td>
</tr>
<tr>
<td>ID Bus</td>
<td>DR</td>
<td>4</td>
</tr>
<tr>
<td>Bypass</td>
<td>DR</td>
<td>1</td>
</tr>
</tbody>
</table>

**BSCAN2 instructions**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Data register</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>11111100 (FC)</td>
<td>ID Bus</td>
<td>SCANIDB</td>
</tr>
<tr>
<td>01111101 (7D)</td>
<td>ID Bus</td>
<td>READIDB</td>
</tr>
<tr>
<td>01111110 (7E)</td>
<td>Select</td>
<td>SCANSEL</td>
</tr>
<tr>
<td>All others</td>
<td>Bypass</td>
<td>BYPASS</td>
</tr>
</tbody>
</table>

**Select register**

The Select Register (SR) is an 8-bit serial register that determines which, if any, of the local scan paths (LSPs) will be active. Assertion of TRST or entry into the Test-Logic-Reset TAP controller state forces all bits to zero. The register is divided into four 2-bit sections, each controlling one LSP. Table 4 shows the SR bits controlling the operation of MSPTMS and MSPTDO.
4-port select register mapping

<table>
<thead>
<tr>
<th>Bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
</tr>
<tr>
<td>PORT</td>
<td>LSP4</td>
<td>LSP3</td>
<td>LSP2</td>
<td>LSP1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Port control via the select register

For Lattice Scan Path linker families consisting of two BSCAN2 macros in a single device, the Select Register Mapping is as below.

<table>
<thead>
<tr>
<th>EN</th>
<th>MS</th>
<th>MSPTMS</th>
<th>MSPTDO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>H</td>
<td>Z</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>L</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>TMS</td>
<td>Active</td>
</tr>
</tbody>
</table>

8-port select register mapping

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Port</td>
<td>LSP4</td>
<td>LSP3</td>
<td>LSP2</td>
<td>LSP1</td>
<td>LSP8</td>
<td>LSP7</td>
<td>LSP6</td>
<td>LSP5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Lattice BSCAN2 chains can be configured in 2 methods

1. Declaring individual Lattice BSCAN2 macros in the device section.
2. Describing Lattice BSCAN2 using PDL (Part Description Library).

Note: In the following sections, we will describe the configuration procedure for a single Lattice device containing two BSCAN2 using the 2 methods mentioned above.

1st BSCAN2 contains the below mentioned chain configuration on each port.

LSP1 := "U261";
LSP2 := "U310";
LSP3 := "U262";
LSP4 := "U265";
LSP5 := "U1";
LSP6 := "U1_1";
LSP7 := "U1_3";
LSP8 := "U162";

2nd BSCAN2 contains the below mentioned chain configuration on each port.

LSP10 := "U2003, U2, U111";
LSP11 := "U1_4";
LSP12 := "U311";
LSP13 := "U3002, U4";
LSP14 := "U188, U444";
LSP15 := "U286, U332, U91";

1st BSCAN2 BYPASS bit will be “U214”
2nd BSCAN2 BYPASS bit will be “U214_1”
Configuring Lattice BSCAN2 Chain Using Method 1: Declaring Individual Lattice BSCAN2 Macros in the Device Section

Procedure: Declare Lattice BSCAN2 programmed into U214 (single Lattice device containing two BSCAN2) into the device section as two separate devices – U214 & U214_1

Step 1
Find “U214” in ‘Device List’ and select/highlight

Step 2
Click on “Copy” and enter the new ‘Device Designator’ as U214_1
Step 3
Device U214_1 is created in the device list as depicted below.

Step 4
Assign the 'lattice-dummy' BSDL (See Appendix 1 for lattice dummy BSDL) for U214 and U214_1.

Note: The lattice-dummy BSDL is declared to U214 and U214_1 to integrate the BYPASS bit for each BSCAN2 macro into the chain. This BYPASS bit appears at the end of each BSCAN2.

Step 5
Select all the boundary scan devices to reconfigure the chain and click on "Join" to link all the boundary scan devices.
Step 6
The Join Chain Devices List appears as below showing the chain sequence.

Join the devices into a single chain following the below rules.

- Insert ‘pad’ bit at the beginning of every LSP of BSCAN2 followed by the boundary scan device order for that particular port
- At the end of all the ports for the BSCAN2 insert the BYPASS bit for that particular BSCAN2 i.e. U214 and U214_1
- Generate the Full chain with Lattice BSCAN2

Step 7
The Chain Graphics depicts the Full chain as below.
Step 8
Generate Full_Chain test by clicking on ‘Generate/Compile’

Step 9
Tests are generated for ‘Full_Chain’
Step 10

Click on a test and in the ‘Insert Source’ ≥ ‘Pre-Test Content’ insert the ISL configuration to enable the two BSCAN2 and all the active LSPs. Scanpath linker

lattice BSCAN2 ISL configuration
SIR 16
TDI(7E7E); !SCAN SELECT which enable two(2) BSCAN2
SDR 32
TDI(AAAA2AAA); !Select/enable Ports 1 to 15

Note: Click on “Apply to All” to have the ISL applied to all the tests.

Step 10. Click on a test and in the ‘Insert Source’ ≥ ‘Pre-Test Content’ insert the ISL configuration to enable the two BSCAN2 and all the active LSPs.
Configuring Lattice BSCAN2 Chain Using Method 2: Describing Lattice BSCAN2 Using PDL (Part Description Library)

Procedure: Declare Lattice BSCAN2 programmed into U214 as Part Description Library with two separate devices for each BSCAN2 - U214 & U214_1

Step 1
Find "U214" in 'Device List' and select/highlight
Declare "U214" as Part Description Library (PDL)

Note: The PDL will expand the U214 into two child devices - "U214%SCAN1" and "U214%SCAN2." Refer to Appendix 1 for U214%SCAN1 BSDL file, Appendix 2 for U214%SCAN2 BSDL file and Appendix 3 for PDL for U214.

Step 2
Generate the chain for all the devices

Step 1. Find "U214" in 'Device List' and select/highlight

Step 2. Generate the chain for all the devices
Step 3
Generate the full chain with pad insert by joining the chain devices in the list following the below rules.

- Insert ‘pad’ bit at the beginning of every LSP of BSCAN2 followed by the boundary scan device order for that particular port
- At the end of all the ports for the BSCAN2 insert the BYPASS bit for that particular BSCAN2 i.e. U214 and U214_1
- Generate the Full chain with Lattice BSCAN2

Step 4
Generate Full_Chain test by clicking on ‘Generate/Compile’

Step 5
Tests are generated for ‘Full_Chain’
Step 6

Click on a test and in the ‘Insert Source’ ≥ ‘Pre-Test Content’ insert the ISL configuration to enable the two BSCAN2 and all the active LSPs

!Scanpath linker lattice BSCAN2 ISL configuration
SIR 16
TDI(7E7E); !SCAN SELECT which enable two(2) BSCAN2
SDR 32
TDI(AAAA2AAA); !Select/enable Ports 1 to 15

Note: Click on “Apply to All” to have the ISL applied to all the tests.
Appendix 1. Lattice-Dummy BSDL for U214, U214_1 and U214%SCAN1

entity Lattice_Dummy is
  -- Generic Parameter
generic (PHYSICAL_PIN_MAP : string := "NONE");

  -- Logical Port Description
port (  
    TCK: in bit; — TCK_0
    TDI: in bit; — TDI_0
    TDO: out bit; — TDO_0
    TMS: in bit; — TMS_0
    GND: linkage bit
  ); —end port list

  -- Use Statements
use STD_1149_1_2001.all;

  -- Component Conformance Statement(s)
attribute COMPONENT_CONFORMANCE of Lattice_Dummy : entity is
  "STD_1149_1_2001";

  -- Device Package Pin Mappings
attribute PIN_MAP of Lattice_Dummy : entity is PHYSICAL_PIN_MAP;
class constant NONE: PIN_MAP_STRING:=
  "TCK:G11," &
  "TDI:H13," &
  "TDO:G14," &
  "TMS:G12," &
  "GND:A5";

  -- Scan Port Identification
attribute TAP_SCAN_IN  of TDI : signal is true;
attribute TAP_SCAN_MODE  of TMS : signal is true;
attribute TAP_SCAN_OUT  of TDO : signal is true;
attribute TAP_SCAN_CLOCK  of TCK : signal is (20.0e6, BOTH);

  -- Instruction Register Description
attribute INSTRUCTION_LENGTH of Lattice_Dummy : entity is 8;
attribute INSTRUCTION_OPCODE of Lattice_Dummy : entity is
  "BYPASS (11111111)," & — BYPASS
  "EXTEST (11110000)," & — DOES NOT EXIST; Defined to satisfy 1149.1
  "SAMPLE (11110001)," & — DOES NOT EXIST; Defined to satisfy 1149.1
  "PRELOAD (11110000)"; — DOES NOT EXIST; Defined to satisfy 1149.1

attribute INSTRUCTION_CAPTURE of Lattice_Dummy : entity is
  "XXXXXXXX01";

  -- Optional Register Description
  -- Register Access Description
attribute REGISTER_ACCESS of Lattice_Dummy : entity is
  "BYPASS (BYPASS)," &
  "BOUNDARY (SAMPLE,PRELOAD,EXTEST)";

attribute BOUNDARY_LENGTH of Lattice_Dummy : entity is 1;
attribute BOUNDARY_REGISTERS of Lattice_Dummy : entity is
  "0 (BC_2, *, internal, 1)";
end Lattice_Dummy;
Appendix 2. Lattice-Dummy1 BSDL for U214%SCAN2

entity Lattice_Dummy1 is
  -- Generic Parameter
generic (PHYSICAL_PIN_MAP : string := “NONE”);

  -- Logical Port Description
port (  
    TCK: in bit; -- TCK_0  
    TDI: in bit; -- TDI_0  
    TDO: out bit; -- TDO_0  
    TMS: in bit; -- TMS_0  
    GND: linkage bit
  ); --end port list

  -- Use Statements
use STD_1149_1_2001.all;

  -- Component Conformance Statement(s)
attribute COMPONENT_CONFORMANCE of Lattice_Dummy1 : entity is
  “STD_1149_1_2001”;

  -- Device Package Pin Mappings
attribute PIN_MAP of Lattice_Dummy1 : entity is PHYSICAL_PIN_MAP;
constant NONE: PIN_MAP_STRING:=
  “TCK:G11,” &
  “TDI:H13,” &
  “TDO:G14,” &
  “TMS:G12,” &
  “GND:A5”;

  -- Scan Port Identification
attribute TAP_SCAN_IN of TDI : signal is true;
attribute TAP_SCAN_MODE of TMS : signal is true;
attribute TAP_SCAN_OUT of TDO : signal is true;
attribute TAP_SCAN_CLOCK of TCK : signal is (20.0e6, BOTH);

  -- Instruction Register Description
attribute INSTRUCTION_LENGTH of Lattice_Dummy1 : entity is 8;
attribute INSTRUCTION_OPCODE of Lattice_Dummy1 : entity is
  “BYPASS (11111111),” & -- BYPASS
  “EXTEST (11110000),” & -- DOES NOT EXIST; Defined to satisfy 1149.1
  “SAMPLE (11110001),” & -- DOES NOT EXIST; Defined to satisfy 1149.1
  “PRELOAD (11110001);” -- DOES NOT EXIST; Defined to satisfy 1149.1

attribute INSTRUCTION_CAPTURE of Lattice_Dummy1 : entity is
  “XXXXXX01”;

  -- Optional Register Description
  -- Register Access Description
attribute REGISTER_ACCESS of Lattice_Dummy1 : entity is
  “BYPASS (BYPASS),” &
  “BOUNDARY (SAMPLE,PRELOAD,EXTEST);”;

  -- Boundary-Scan Register Description -- DOES NOT EXIST; Defined to satisfy 1149.1
attribute BOUNDARY_LENGTH of Lattice_Dummy1 : entity is 1;
attribute BOUNDARY_REGISTER of Lattice_Dummy1 : entity is
  “0 (BC_2, *, internal, 1)”;
end Lattice_Dummy1;
Appendix 3. Lattice BSCAN2 Part Description Library

! This is the part library for lattice Linker BSCAN2. 16 port

library "SCAN1", nr, ns, pn"lattice_lib", scan, ts"1149_1", bsdl"lattice-dummy", pkg"NONE"
library "SCAN2", nr, ns, pn"lattice_lib", scan, ts"1149_1", bsdl"lattice-dummy1", pkg"NONE"

external pins "B13"
    device "SCAN1" pins "B13"
external pins "E11"
    device "SCAN1" pins "E11"
external pins "E10"
    device "SCAN1" pins "E10"
external pins "K12"
    device "SCAN1" pins "K12"
external pins "D11"
    device "SCAN1" pins "D11"
external pins "G11"
    device "SCAN1" pins "G11"
external pins "G12"
    device "SCAN1" pins "G12"
external pins "G14"
    device "SCAN1" pins "G14"
external pins "H13"
    device "SCAN1" pins "H13"
external pins "A14"
    device "SCAN2" pins "A14"
external pins "A13"
    device "SCAN2" pins "A13"
external pins "C12"
    device "SCAN2" pins "C12"
external pins "C11"
    device "SCAN2" pins "C11"
external pins "B12"
    device "SCAN2" pins "B12"
From Hewlett-Packard through Agilent to Keysight
For more than 75 years, we’ve been helping you unlock measurement insights. Our unique combination of hardware, software and people can help you reach your next breakthrough. Unlocking measurement insights since 1939.

myKeysight
www.keysight.com/find/mykeysight
A personalized view into the information most relevant to you.

Keysight Infoline
Keysight’s insight to best in class information management. Free access to your Keysight equipment company reports and e-library.

Keysight Channel Partners
www.keysight.com/find/channelpartners
Get the best of both worlds: Keysight’s measurement expertise and product breadth, combined with channel partner convenience.

myKeysight
www.keysight.com/find/mykeysight
A personalized view into the information most relevant to you.

Keysight Infoline
Keysight’s insight to best in class information management. Free access to your Keysight equipment company reports and e-library.

Keysight Channel Partners
www.keysight.com/find/channelpartners
Get the best of both worlds: Keysight’s measurement expertise and product breadth, combined with channel partner convenience.

www.keysight.com/find/x1149

For more information on Keysight Technologies’ products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

Americas
Canada (877) 894 4414
Brazil 55 11 3351 7010
Mexico 001 800 254 2440
United States (800) 829 4444

Asia Pacific
Australia 1 800 629 485
China 800 810 0189
Hong Kong 800 938 693
India 1 800 11 2626
Japan 0120 (421) 345
Korea 080 769 0800
Malaysia 1 800 888 848
Singapore 1 800 375 8100
Taiwan 0800 047 866
Other AP Countries (65) 6375 8100

Europe & Middle East
Austria 0800 001122
Belgium 0800 58580
Finland 0800 523252
France 0805 980333
Germany 0800 6270999
Ireland 1800 832700
Israel 1 809 343051
Italy 800 599100
Luxembourg +32 800 58580
Netherlands 0800 0233200
Russia 8800 5009286
Spain 800 000154
Sweden 0200 882255
Switzerland 0800 805353
Opt. 1 (DE)
Opt. 2 (FR)
Opt. 3 (IT)
United Kingdom 0800 0280637

For other unlisted countries:
www.keysight.com/find/contactus

DEKRA Certified ISO 9001:2008
www.keysight.com/go/quality
Keysight Technologies, Inc.
DEKRA Certified ISO 9001:2008
Quality Management System

www.keysight.com/find/service
Keysight’s insight to best in class information management. Free access to your Keysight equipment company reports and e-library.

www.keysight.com/find/x1149

This information is subject to change without notice.
© Keysight Technologies, 2015
Published in USA, October 30, 2015
5992-1045EN
www.keysight.com