Keysight Technologies
Increase PA/FEM Component Test Efficiency with MIPI® RFFE and SPI Bus Test Techniques

Application Note
RF power amplifiers (PAs) and front end modules (FEMs) are essential for modern wireless device operation. PA and FEM components, including PAs, LNAs, tuners, filters and switches, typically include a serial bus interface to support reconfigurations for power and band settings. As the variety of RF protocols increases so do the demands on the PA/FEM components and RFIC to PA/FEM communications. To better address these serial communications, the MIPI® alliance has developed the RF front end interface (RFFE) specification. The MIPI RFFE communications bus standard provides both PA/FEM suppliers and users a common serial communications framework to build on.

Validating RFFE communication robustness for new PA/FEM components includes basic communication validation for PA/FEM control, as well as extensive bus timing and logic level margin testing. Methods to characterize and validate PA/FEM serial bus performance and IO pin parametric performance are described in this application note. RFFE interface test is the primary focus, although the general concepts apply to other master/slave serial bus configurations including SPI.
PA/FEM RFFE IO Test Considerations

The MIPI RFFE communications interface is a fast and efficient 2-wire serial bus that runs in a master/slave configuration. A master RFIC device controls either a single or multiple PA/FEM slave devices. RFFE v1.0 devices operate at standard clock rates up to 26 MHz, while RFFE v2.0 extends clock rates up to 52 MHz. The bus master provides the clock (SCLK) to the slave devices, and the RFFE data bus (SDATA) supports bi-directional IO allowing slave devices to provide in-frame responses during Register Read Command Sequences (CS). RFFE physical layer attributes described in the RFFE specification include logic levels, interconnect impedances, clock and data slew rates, as well as methods to provide power for IO circuitry using the RFFE VIO line. RFFE v2.0 added the extended clock rates to 52 MHz as well as CS multi-rate support. In addition, v2.0 adds multiple master support which allows the RFIC Bus Owner Master (BOM) to transfer master role to a secondary RFIC master device. RFFE v2.0 also provides methods for slave device interrupts using a polling mode as well as a slave triggering for time critical applications. Details on MIPI RFFE interface bus may be found at the MIPI RFFE specification site www.mipi.org.

PA/FEM component design validation test (DVT) requires test instrumentation which can operate in the RFFE master role. Commercially available digital pattern stimulus/response (DSR) products with PMU support (parametric measurement unit) may be used if the DSR is carefully selected. Key requirements for PA/FEM RFFE test instrumentation include:

- Bi-directional bus support: RFFE bus test requires DSR products that can support bi-direction bus transactions beyond 52 MHz. The high bus rate and bi-direction bus requirement mean DSR sequencers must be hardware state machine controlled and capable of bus input/output direction change in one bus cycle.
- Edge timing control: Methods for seamless configuration of clock-to-data edge placements and multiple clock rate support is critical for time margin testing.
- Programmable logic level control: Logic level drive and threshold levels must be controllable for specific bus level implementations as well as level margin test.
- Support for long fixture lines and flexible DUT response terminations: Fixturing for DVT may result in cables that are long enough that the cable propagation time is significant compared to the bus data period (19 ns at 52 MHz). Methods to compensate for this and program receiver terminations are necessary.
- Fast time to test deployment: Short PA/FEM design cycles means quick DVT development time is a must. The DSR solution must be architected for reusability and ease-of-use, leading to quick test development and deployment.
- Flexible support of non-standard implementations: Prototype PA/FEM components may not fully meet the RFFE standards in either the command sequences or physical layer. The DSR solution needs to be flexible to support non-standard implementations.
Using a PXIe Digital Stimulus/Response for PA/FEM Test

The Keysight Technologies, Inc. M9195B Digital Stimulus/Response (PXI DSR) unit is ideal for PA/FEM design validation test. The PXI DSR was architected for quick pattern setups, flexible clock speeds and user programmable clock-to-data edge timing and logic level values. Serial bit-streams are easily constructed using either legacy bulk data (text based vector files) or by on-the-fly command sequence download at run time using PXI DSR’s unique set signal feature. Once the pattern is downloaded to the PXI DSR internal memory, both signal timing and logic attributes may be quickly modified using API methods allowing for fast and efficient margin testing.

The PXI DSR has 16 bi-directional channels – each channel is capable of operating in either a dynamic digital pattern mode or a parametric measurement mode. When used in the dynamic pattern mode the 16 channels are capable of high speed pattern generation and acquisition with pattern rates up to 250 MHz and independent vector by vector direction control. When used in parametric measurement mode each channel provide DC source/measurement features useful for IO leakage current and protection clamp verification.

STIL Components and Architecture

Fast test development and deployment is essential for PA/FEM DVT. The PXI DSR architecture, terminology and programming methods are based on the IEEE standard 1450 Standard Test Interface Language (STIL) specification. The intuitive terminology and methods to describe pattern attributes make STIL a natural choice for use with the PXI DSR.

Patterns are constructed from building blocks, collectively referred to as STIL components. STIL components are driver objects, dynamically created and defined by either importing a text based STIL file, an Open XML file (Microsoft Excel) or created programmatically using the PXI DSR instrument driver. A STIL component programming model is very flexible and results in easier pattern setup, debug and re-usability allowing quicker DVT system deployment.
Digital Timing-Sets, Waveforms and Edge Placement

Serial bus IO is generated using the PXI DSR in digital pattern mode, with each bit in the bit-stream corresponding to a vector in the pattern. The PXI DSR uses a vector cyclizer which enables the user to program multiple events within each vector period, also known as a vector waveform. Up to two drive events and one response event are permitted in each vector period. The multi-event vector waveform capability allows simple generating of return to zero (RTZ) encoding, greatly improving usability, memory utilization and ease of programming. Instead of oversampling the pattern to generate a clock (a common method with many HSDIO/DSR products) the PXI DSR can directly generate RTZ clocking.

The timing placement of the events within the period is user settable with up to 1 ns resolution, and can be modified bit-by-bit which works well for timing margin test. The PXI DSR also support precise channel-to-channel timing offsets programmable in 25 ps steps – useful for precision timing setup and hold time tests.

The PXI DSR separates timing-set and pattern data entry which enables multiple applications of the same pattern with different timing sets. This feature allows extremely fast re-apply of patterns with various timing sets for thorough timing analysis. The timing-set information is contained in a STIL component known as a waveform table. Up to 32 waveform tables may be defined and assigned to patterns on a vector-by-vector basis.

One example demonstrating the advantage of multiple waveform table support is RFFE v2.0 Half-Speed Data Response (HSDR) operation. HSDR may be accomplished by simply assigning the appropriate waveform table to the command sequence vectors which will cause them to run at the half-speed rate. The RFFE command sequence timing will seamlessly change from full rate to half rate with no gaps or glitches and there is no need to modify the pattern itself.

Methods for On-the-fly Modifications and Re-Evaluations

Timing sets, pattern contents and logic levels may be re-evaluated at run time (after the pattern data has been downloaded to the PXI DSR memory). By only modifying the essential memory objects as required command sequences may be modified and re-applied very quickly. The PXI DSR supports specific API’s for manipulating pattern and timing attributes residing in its hardware memory:

- Modify signals and vectors in the pattern memory: The SetSignal programming method may be used to directly change only the SDATA Command Sequence pattern memory. This approach results in a very low RFFE command latency.
- Modify waveform tables on a vector by vector basis: The SetWaveformTable programming method assigns waveform tables to individual vectors. This is used for quick serial bus clock rate changes or vector edge time changes.
- Modify timing variables: The ReevaluateVariables programming method operates on variables present in waveform timing tables. These variables can be used to modify vector edge placement or period.
- Re-evaluate logic (DCLevel) variable: The ReevaluateDcLevels programming method operates on variables present in the DCLevel STIL Component block, which allows fast setups of logic levels.
Site Definitions: Map and Grouping of Channels to DUT Pins

The PXI DSR channels are logically grouped into blocks known as sites. The site block maps physical channels to the DUT. This approach allows re-mapping as needed when the fixture changes or when expanding to a multi-DUT test setup.

Multiple sites can be defined and they may even contain overlapped channels. At activation time the sites are associated with a mode of operation – either dynamic pattern or PMU measurement mode. A DVT test is executed by activating and deactivating sites as needed in either dynamic digital or PMU mode.

DUT Serial IO Response Considerations

In RFFE test applications the DUT may provide a response during RFFE read Command Sequence. In those cases the transmission line propagation times and response receiver terminations (on the instrument side) become a factor. It is desirable to keep the distance from the DUT to instrumentation as short as possible, although in some cases a meter or more may be unavoidable. The PXI DSR provides a response delay compensation, which allows a time offset between the pattern source and the response clock. This time offset can place the response strobe precisely where needed to clock in the DUT response. Even for RFFE extended rate (up to 52 MHz) DUT responses can be reliably captured.

The PXI DSR also has various receiver termination modes to accommodate DUT requirements.
- High impedance response termination: during DUT response bits the PXI DSR channel is instantaneously set to a high impedance state. This is the most common termination method in test systems.
- 50 ohm response termination: if the DUT is capable of driving a 50 ohm load the transmission line may be terminated into 50 ohms at the receiver for best signal fidelity.
- Active load termination: The PXI DSR receivers have high speed current switches capable of terminated a DUT response with programmable current load up to ±20mA. The active termination may be used to verify the DUT output level can be achieved under specific load conditions. The active termination can also be used to provide a pull-down current when necessary.

IO Pin Parametric Test

PA and FEM design validation tests usually include DC parametric testing as well. IO pin continuity, isolation, leakage and protection clamp circuit checks are all examples of DC based parametric tests which may be necessary. The PXI DSR includes a built-in pin parametric measurement unit (PPMU or PMU), which provides the essential force current measure voltage (FIMV) and force voltage measure current (FVMI) measurement capability on each channel. Voltage compliance and current limiting may be set to protect valuable prototypes. The PXI DSR also supports remote voltage sense to remove cable effects when sourcing higher currents.
VIO Power Considerations

The RFFE specification has provisions for powering the PA/FEM serial IO circuits using the VIO line. The current required by each PA/FEM device is relatively low – typically less than 1.25 mA. During RFFE read command sequences the DUT instantaneous current may be higher since the SDATA driver may source current to charge transmission line capacitance. The PXI DSR channels may provide VIO power using either PMU mode or pattern mode.

In PMU mode the PXI DSR provides up to 40 mA of current with low source impedance. If the VIO instantaneous current draw is more than a few mA's it is recommended using a PMU channel to source VIO current.

In pattern mode the PXI DSR may also provide VIO current via output drivers, despite having a nominal 50 source resistance. This means the source voltage will drop slightly as VIO line draws current. If DUT VIO instantaneous currents are < 1 mA, a channel in pattern mode may be used to source VIO. Otherwise use the PXI DSR PMU mode of operation for VIO power.

Serial Bus Programming Methods and Test Flow Using the PXI DSR

The PXI DSR supports multiple programming methods to construct RFFE commands for different test applications and requirements. The primary programming methods used for RFFE command generation include:

- Bulk data import: User provided pattern files are imported and used to generate I/O command frames. Bulk data files contain pattern information in the form of ASCII text, and pattern information is encoded with characters such as 1, 0, Z, H, L or X to represent the logic drive or expected response states.
- On-the-fly CS generation: The most flexible programming method uses the PXI DSR Set-Signal feature to define commands at run-time. This provides a natural "on-the-fly" programming flow which is particularly useful when the command contents change from DUT to DUT (such as serial numbers, date code and amplifier trim values).

Both of these programming methods may be used in a test plan. For example, during early portions of the test, large blocks of command sequences may be imported using bulk data. Later during the test, on-the-fly programming methods may be used to set-up run-time generated information such as trim values, date codes and serial numbers. The following sections provide more detail on each programming method.
Bulk data import

Bulk data files are first imported to the PXI DSR driver (software) memory. Since the files themselves only contain pattern information and optionally signal names, they must be combined with other pattern attributes using the IVI driver. Information to be combined with the pattern data includes site information (physical channel mapping), logic level information and specific waveform timing information. Once all the attributes for pattern generation is define the pattern is downloaded to “cache memory”, which means it resides in PXI DSR’s hardware memory. This is done to improve speed of test execution.

It is important to note the bulk data could be encoded with a RTZ or RZ clock encoding. Either format is acceptable and can be accommodated at import time by declaring and using an appropriate waveform timing table.

Programming flow for bulk data import and generation is shown in figure 2.

```c
// Load Bulk data:
// BulkData_RZ & BulkData_NRZ have WFT tables associated at load time

string BulkDataRZ_FileName = "RFFE_BulkDataRZ.txt";
string BulkDataNRZ_FileName = "RFFE_BulkDataNRZ.txt";
M9195B.PatternFile.LoadBulkData(BulkDataRZ_FileName, "RFFE_RZ_BulkData", ",", "WFT_RFFE");
M9195B.PatternFile.LoadBulkData(BulkDataNRZ_FileName, "RFFE_NRZ_BulkData", ",", "WFT_RFFE_NRZ");
```

Bulk data files do not contain timing information and are associated with timing information at import time. Also, site information is specified prior to run time.

Figure 2. Bulk data ASCII files are imported using LoadBulkData method.
On-the-fly programming

To program using the on-the-fly method, first create a serial IO pattern template as shown in figure x. The pattern is imported to the PXI DSR’s driver memory, combined with other pattern attributes (site, logic level and timing information), and then downloaded to “cache memory”. At run time, the “set signal” API is used to modify the pattern in memory per the specific command required at that time (figure 3). The pattern memory is modified starting at the previously defined label. Once modified, the command is generated by issuing an initiate command. Using this approach allows low latency command construction and generation in a flexible programming module. Programming flow for Set Signal style programming is shown in figures 4 and 5.

Figure 3. On-the-fly programming step 1: Configure pattern memory template for serial IO. The specific content is not critical since the pattern will be updated at run time.

Figure 4. On-the-fly programming step 2: At runtime update pattern memory as needed.
Pattern Margin Testing Using Re-Evaluations and Stimulus Delays

Once the pattern and timing set information is downloaded to the PXI DSR, extensive DUT timing and logic level margin testing may be quickly executed. The PXI DSR supports variable re-evaluation for both waveform timing and logic levels. Figure 6 shows impacts of re-evaluating the waveform timing table for edge placement and how that may be used for RFFE command margin testing. The SDATA edge may selectively be moved with respect to SCLK until the DUT generates an error. Using re-evaluation to modify edge placement provides vector by vector edge timing placements with up to 1 ns resolution.
An alternate method for channel-to-channel margin testing, the stimulus delay setting acts on the channel and impacts the edge settings for all the vectors in the pattern. Figure 7 shows how SDATA can be set relative to SCLK as captured with an infinite persistence scope. In this case, SDATA is moved in 200 ps steps.

![Figure 7](image1.png)

Figure 7. Use PXI DSR stimulus delay place SDATA edge relative to SCLK. Infinite persistence scope displays multiple acquisitions, demonstrating edge placement resolution.

RFFE bus logic levels may also be changed as needed using the ReevaluateDclevels API. As shown below using an infinite persistence scope capture the applied logic levels have been stepped in 100 mV increments.

![Figure 8](image2.png)

Figure 8. ReevaluateDclevels may be used to step logic levels.
Summary

PA and FEM DVT utilizes a digital stimulus/response unit for thorough RFFE serial interface test. Serial command sequence voltage and timing margin test is done to validate operating margin and IO pin leakage and clamp performance needs to be characterized.

The M9195B PXI DSR with PMU provides essential features for fast paced PA/FEM design cycles. The PXI DSR’s STIL component architecture makes pattern attribute programming intuitive and supports quick test development. The architectures separate pattern and timing-set organization allows complex pattern re-applications using various timing scenarios for quick and complete verifications.

Vector waveform cyclizer support with the ability to program multiple drive events within each vector greatly simplifies RTZ and RZ programming. The 1 ns edge placement resolution allows vector by vector edge adjustments for setup and hold margin testing.

Run time pattern modifications and variable re-evaluations allow changes to pattern, timing and logic levels by only changing the necessary attributes resulting in fast and versatile setups.

The site definition block provides convenient method to re-map DUT signals to PXI DSR’s channels, supporting quick fixture change-over and test expansion to multiple DUT’s.
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