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Making Boundary Scan Easy

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Making Boundary Scan Easy

Testing boundary scan devices no longer need be a laborious task.

IT HAS BEEN 20-plus years since the IEEE 1149.1 standard, commonly known as boundary scan or JTAG, came into existence. The boundary scan test method provides a means to electrically test the interconnection between two semiconductor devices equipped with boundary scan, and even devices without boundary scan, such as memories (DDR/Flash) and connectors, without the need for a test probe on every device pin.

High-speed devices and smaller sizes have robbed PCBs of the necessary test points for effective ICT. Integrating boundary scan with ICT provides a good option to overcome limited access test challenges. Some of the methods considered are functional tests, built-in self tests (BIST) and boundary scan. Of the suggested test methods, boundary scan tests are still the easiest and preferred method, as they can be easily integrated with ICT. The following reasons support adoption of boundary scan:

1. Most semiconductor devices (CPLD, FPGA and ASIC) now have boundary scan capabilities.
2. Increased awareness and boundary scan training.
3. Board designers and NPI test engineers are working together to implement boundary scan design for test (DfT).
4. Tools and applications have improved tremendously to ease boundary scan test implementation.

The good news of late is that boundary scan tools and software applications are playing a big role in its successful implementation, from board design to mass production. Let's look at new tools and techniques available to make test development and implementation of boundary scan test easier:

1. Boundary scan software interfaces are equipped with step-by-step guides for developing tests. Engineers no longer have to remember complex commands and flow of the test development.
2. Built-in software automatically assigns the correct BSDL and libraries to devices by referencing part numbers of the devices as declared in the BoM. In the past, engineers had to spend hours on this tedious matching process.
3. New boundary scan software applications are capable of discovering the boundary scan device chain connections of the devices. Test engineers no longer need to go through the hard task of looking in the schematics to find what devices are connected into the boundary scan chain.
4. BSDL and other compilation errors are well documented to help engineers correct them.
5. Software automatically generates the boundary scan test. Software can come with intelligence to analyze board connections and identify pins and devices that are testable, and devices that need to be disabled so that they will not cause bus contention during boundary scan test.
   a. Any changes to the board data, such as editing the BSDL or libraries, or changing the device information,

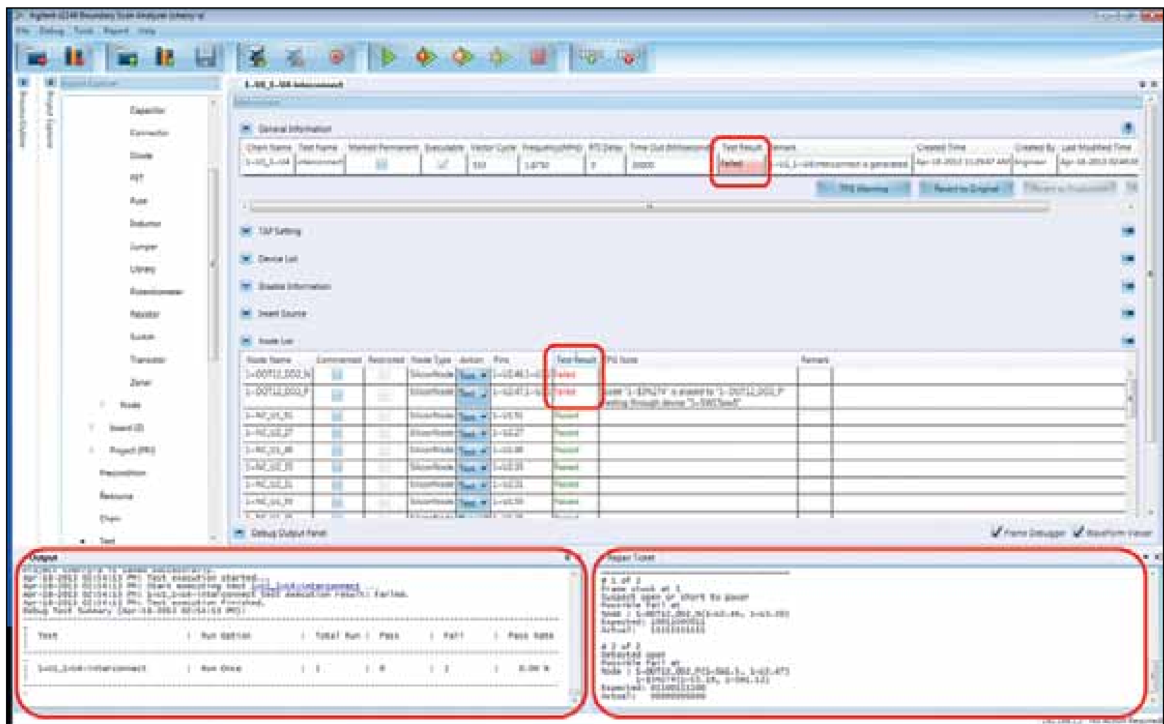

FIGURE 1. Debug interface shows location of failing pins and test during boundary scan interconnect test.

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will trigger the software's internal validation process to analyze if the changes require regeneration of the boundary scan test.

6. Numerous boundary scan debugging tools available help test engineers debug failing tests. FIGURE 1 is an example of a typical debug interface with a message clearly showing the failing device pins for the test engineer to take action.

   Visual GUIs, such as waveform viewers (FIGURE 2), help visualize the TDO signal and compare the failing and passing signals. These waveforms can also identify the devices where the pins are failing during boundary scan interconnect test.

   Other tools show the actual and expected signatures of the boundary scan cells. This will help analyze whether a failure is related to the BSDL or to the boundary scan cell inside the device. This can also reveal whether the failure is caused by pins shorted to a fixed node.

7. Some boundary scan test vendors have proprietary tools to enable coverage enhancements. For example, the silicon nail test is a boundary scan test that makes use of the boundary scan cell to drive and receive signals to and from a target non-boundary scan device. The software application automatically generates a test for that device if the user identifies it as silicon nail and a library is available.

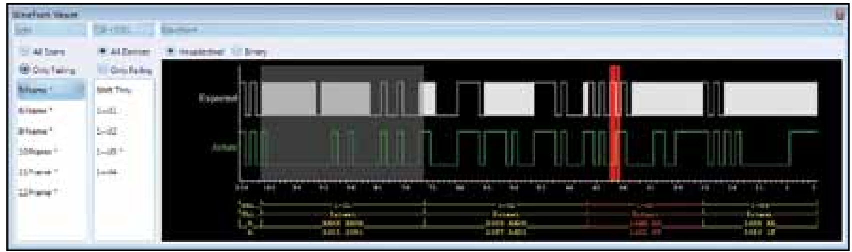

FIGURE 2. Waveform viewer showing the TDOs failure and device that failed during the boundary scan test interconnect.

Other novel tools use a combination of boundary scan and vectorless test method wherein the boundary scan device pins are used as drivers to a non-boundary scan device connected to it. The vectorless sensor and amplifier will detect the capacitance between the sensor plate and the non-boundary scan device, which can be a semiconductor device or a connector.

Gone are the days of laborious test development. There are also various options to help recover test coverage by integrating boundary scan into more traditional in-circuit testers that otherwise would be unable to test highly complex PCBs. As boundary scan continues to garner wider adoption, the industry is likely to see even more applications being developed to make it a common solution. **CA**

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