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Testing of Small Form-Factor Products

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This article was first published in Circuits Assembly, Printed Circuit Design and Fab in August, 2013. Reprinted with kind permission from UP Media Group.

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Published in USA, February 3, 2016
5992-1330EN

Testing of Small Form-Factor Products

Boundary scan and embedded test will need to make up for ICT gaps.

SMALL FORM-FACTOR (SFF) mobility products have spurred massive on-chip integration of CPU, graphics, memory, and multiple communication standard interfaces, ranging from wired to wireless onto a single system-on-chip (SoC) package. The printed circuit board assemblies of these products are extremely dense with memory and storage components soldered down, eliminating bulky connectors to fulfill the "thin" features. PCBs for SFF mobility products pose new manufacturing challenges such as package-on-package SMT assembly and limited real estate for test pads. Diminishing accessibility to probe circuit nets for testing, debug and diagnostics requires a test strategy rethink and updated design for test (DfT) guidelines.

A typical PCB for such SFF products will be littered with 01005 component packages, and the SoC is most likely a BGA with over 1,000 solder balls below the package. The SMT process will benefit from using the full range of AOI equipment:

- Solder paste AOI to eliminate excess and insufficient solder, reducing risks of shorts and opens.
- Pre-reflow AOI to ensure there is no missing, extra or wrong oriented component(s).
- Post-reflow AOI to monitor the performance of the reflow oven and inspect for shorts and opens of visible joints.

While automatic x-ray inspection can inspect hidden solder joints, especially under SoC BGAs and any PoP, implementation is cost-prohibitive.

After SMT, the PCBA risks are shorts and opens on hidden solder joints (if AXI is not implemented) and powered shorts. Electrical test will need to provide test coverage for these gaps.

It is inconceivable to design a board with no test access, as power (all on-board voltages) and ground need to be validated, especially when diagnosing board failures. Together with the power and ground nets, critical signals like inputs, outputs and control lines should be given test access for the same reasons. This is the minimum test access to assess PCB functionality. Test access enables the process of elimination to find the root cause of a failure; generally more test access is preferred to less.

Diagnosing and identifying the defect within the PCBA will need to focus on key components like SoC and memory. Most SoC are IEEE 1149.1 (boundary scan) enabled, and access to its test access port (four nets) expands shorts and opens test coverage to its thousands of hidden solder joints. Boundary scan is a very efficient and productive test methodology for large pin count BGAs. Innovative boundary scan test extensions increase test coverage to components connected to the SoC. These components can be memory, storage, communication and sensor hubs.

Some SoC suppliers like Intel offer proprietary test technology for Haswell microarchitecture CPU designs. Intel SVT, for instance, enables test of the Haswell SoC CPU, its functions and connectivity to the surrounding peripheral components through a custom debug port (12 nets and four nets for boundary scan TAP). It is extremely effective for SFF designs constrained by real estate or high-speed signal fidelity.

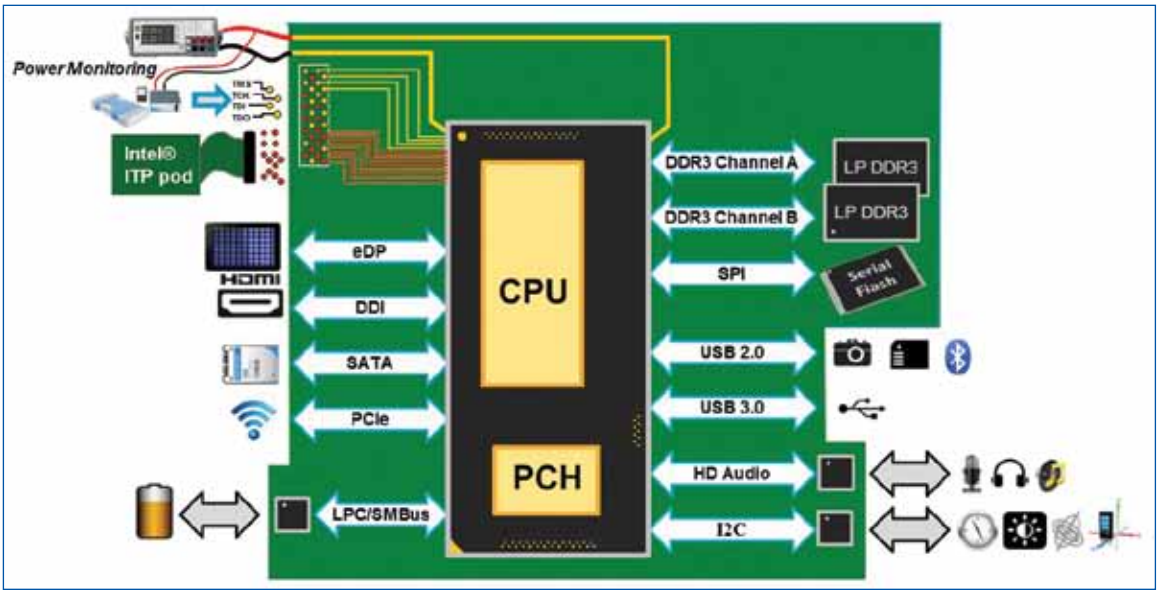

FIGURE 1. Illustration of Intel SVT test coverage.

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Using Intel SVT as an example of SoC embedded testing, test coverage can be extended to (FIGURE 1):

- Platform hub controller (PCH).
- Memory.
- Graphics; e.g., VGA, HDMI, eDP.
- High-speed I/O (HSIO); e.g., PCIe, SATA, USB3.
- Communication interfaces; e.g., LAN, USB2.
- I/O peripherals; e.g., keyboard, audio.

Intel SVT requires the BIOS to reserve a designated register to host the results of the Intel SVT test. During manufacturing test, the PCB under test has to be powered safely to run the BIOS, and Intel SVT will post the results of its test into the designated register. The register content is then compared to known-good-board values to assess whether the PCBA passes or fails the set of tests. Embedded test from other SoC suppliers will be similar.

Implementing SoC embedded test will require adapting the firmware to accommodate embedded testing, similar to Intel SVT requiring the modification of the BIOS.

The DfT guideline for SFF products should resemble these recommendations:

Assumptions:

- Solder paste AOI to eliminate excess and insufficient solder and reduce risk of shorts and opens.
- Pre-reflow AOI to ensure no missing, extra and incorrectly oriented components.
- Post-reflow AOI to monitor reflow oven performance and inspect for shorts and opens of visible joints.

Assignment of test pads for the following (in order of priority):

1. Power nets. Individual test pad for all on-board voltages.
2. Ground nets.
3. Board (I/O) input, output and control signals.
4. TAP (TMS, TCK, TDI & TDO) for all boundary scan components.
5. Debug port(s) of SoC if embedded test is available.
6. All critical signals. Minimally to test for shorts and opens and if sufficient, to test for critical components.

If board real estate for test pads is a concern, alternative test access methodology can be deployed to recover test access. Some alternatives require almost no additional real estate and can be placed on high-speed traces without affecting signal fidelity.

The manufacturing test for SFF products will have elements of in-circuit test, boundary scan and, if available, the SoC supplied embedded test. ICT will be deployed for all accessible nets to eliminate open/short defects on the accessible nets, and if sufficient test access is granted, test for critical components. The manufacturing test strategy is illustrated in TABLE 1.

Boundary scan and embedded test will most likely require fewer than 20 probes, and the equipment to perform the tests is a PC controller (or a notebook PC) with a boundary scan box, benchtop power supply, cables and connectors. This test can easily start its life in an R&D lab on prototype boards and then be reused in its entirety in manufacturing, either as a separate standalone station or incorporated with ICT.

The objective of an SFF product manufacturing test strategy is to optimize test coverage and provide useful diagnostics to enable efficient repair with minimal test accessibility. ICT has been the *de facto* test deployed in manufacturing. Diminishing test access in SFF will reduce its effectiveness. The loss of ICT coverage and diagnostics has to be recovered by the addition of boundary scan and embedded test. CA

TABLE 1. Manufacturing Test Strategy for SFF Products

Metrology	Test	Comment
In-Circuit	Open / Short	Net access dependent
		1. Power(all on-board voltages) & Ground
		2. Input, Output & Control signal
		3. Boundary Scan TAP
		4. Debug port(s) of SoC (if embedded test is available)
		5. All other critical signals
	Analog device	Net access dependent
	Power-up	Voltage monitoring of all on-board voltages
	Digital device	Net access dependent
Boundary Scan	Power Monitor	Voltage monitoring of all on-board voltages
	Interconnect	Open / Short on all Boundary Scan components
	Interconnect	Device ID to verify correct component
	Interconnect	Loop Back tests
	Silicon Nail	Components connected to Boundary Scan components
	Cover-Extend Test	Connectors connected to Boundary Scan components
Embedded Test	Initialize	Initialize SoC for embedded test
	SoC ID	Verify SoC component information
	SoC tests	All embedded tests provided by SoC supplier