The automated scan path linker configuration feature introduced with the release of software version 1.6.0.0 simplifies scan path linker configuration for five scan path linker devices commonly used in the industry.
Introduction

A boundary scan linker mux (multiplexer) device, also known as JTAG scan bridge or scan path linker, is a device that will be able to link or join multiple boundary scan chains into one single chain or multiple chain configurations, depending on how the boundary scan linker mux device is configured. This application note describes how to configure scan path linkers using the new automated scan path linker configuration feature introduced in software release 1.6.0.0 for Keysight Technologies x1149 Boundary Scan Analyzer.

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The Function of Scan Path Linkers

Figure 1 below shows a typical boundary scan linker connecting multiple chains. Nesting of chains on multi-board configurations can be simplified by nested scan path linkers (as depicted in Figure 2) provided, where scan path linkers are used to configure a chain of multiple boards.

Figure 1. The boundary scan linker mux device U1 joins Chain 1, Chain 2, Chain 3, Chain 4 and Chain 5.

We can achieve better management and flexibility of boundary scan chain in the testing of complex designs using a CPLD as a scan path linker. A scan path for each circuit (CPU block, Data Processing block, IO management, Memories, etc.) provides a means to control the TAP signals independently.

Figure 2. Nested scan path linkers.
**Challenges**

Manual configuration of scan path linkers is a complex process that requires in-depth understanding of scan path linkers. It involves understanding the details of registers, the method of configuring these registers and the order of invoking instructions to enable the configuration.

This time-consuming process is compounded by the wide range of devices in the market which users need to familiarize themselves with in order to correctly configure.

**Solution**

The automated scan path linker feature introduced in the Keysight Technologies, Inc. x1149 software version 1.6.0.0 simplifies configuration by automatically configuring the parameters for the selected scan path linker device.

**Overview of Automated Scan Path Linker Configuration**

The new feature supports the following Scan Path Linkers.

- Texas Instrument - Scansta 112
- Firecron JTX05, JTX07, JTX09
- Lattice BSCAN FPGA

The Lattice, ScanSta and JTX libraries can be found as standard libraries in the software with the following file names.

<table>
<thead>
<tr>
<th>Scan path linker</th>
<th>File name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lattice</td>
<td>Lattice_SPL.bsdl</td>
</tr>
<tr>
<td>ScanSta</td>
<td>ScanSta_SPL.bsdl</td>
</tr>
<tr>
<td>JTX</td>
<td>JTX05_SPL.bsdl, JTX07_SPL.bsdl and JTX09_SPL.bsdl</td>
</tr>
</tbody>
</table>
Applying an automated scan path linker to a test

1. Create a new project:
   - Add board under the Board List tab.
   - Import board
2. Scan Path Linker device definition

In the Device List, select the Device Designator of the scan path linker. From the On Board Linker (OBL) drop-down menu, select the scan path linker type according to the device used in the project to map the library that corresponds to the device.

The details of the device can also be entered using the Edit Device - Library function. Right click on the Device Designator to expand the menu and select Edit Device.
Figure 7. Editing scan path linker device properties.
3. Configure chains

Configure individual sub-chains that will be used in the scan path linker. Individual sub-chains detected are shown in the **Chain List**.

- Select all the individual chains that are part of the scan path linker and click on **Join** to create a scan path linker chain. The ports for the OBL devices (Scan Path Linker) are created automatically. The number of ports depend on the OBL device type.

![Figure 8. Scan path linkers sub-chains detection.](image)

![Figure 9. Configuration of scan path linker chain.](image)
- As seen in Figure 10, you can map a single chain to a port by dragging the chain onto the port.

![Figure 10. Drag and drop single chains to scan path linker ports.](image)

- Ensure that all the single chains are mapped.

![Figure 11. Configured scan path linker.](image)
- A □ indicates a front pad will be added in front of the port during OBL chain creation. To insert or remove the front pad in a port, click on Insert Pad or Remove Pad, as shown in Figure 12 and 13.

- If required, you can add or remove the back pad □ by right-clicking the port and selecting Insert Back Pad.

Figure 12: Pad Removal

Figure 13. Back pad insertion
Figure 14 shows you how to select the position of the OBL device during chain creation. If the option **Position OBL device in front** is not selected, it will be placed at the end during chain creation.

4. Complete the configuration

- Click OK to complete the scan path linker chain configuration. Once the sub-chain mappings are complete, the chain graphics below along with automated **Pre-Test Content** are generated to control the scan path linker.

![Figure 14. Position OBL device in front selection.](image)

![Figure 15. Pre-test content generation in chain configuration.](image)
Test Generation

Once the chain configuration is successfully completed, the project is ready to generate tests.

Figure 16. Scan path linker test generation.
Pad Bit

Pad bits are like Bypass registers along each scan port. Similar to the way we enable Bypass of a device using Bypass instruction, the scan path linker can be configured to bypass a scan port from the chain without the need to physically rework the board.

By default, a pad is added to each port before the first device of the chain on that port. This can be removed if the scan path linker is programmed to not have the pad or, if the pad is added at the end of the last device of the chain.
Depiction of Front and Back Pads

Front pads are indicated in light blue in the application as shown in Figure 18.

Back pads are indicated in orange as shown in the application as shown in Figure 19.

Positioning Scan Path Linkers (OBL devices) in a Chain

Scan path linkers are BSCAN devices. The TAP controller of scan path linkers can daisy chain and enable it as an entity in the test for a chain. A scan path linker can be positioned as the first device of the entire chain or the last device depending on how it is programmed. By default, it is set as the last device. If programmed as first, you can easily modify the position in the software as the first device of the chain, shown in Figure 20.
Multiple-Core Device

A multiple-core device is defined as separate devices (one device definition for each core) by the software during scan path linker chain configuration. The software automatically combines them into a single device, with double the number of ports. For example, in Figure 21, MB has a single device U100 which contains 2 cores of scan path linker segmented at 8 port boundary. This is divided virtually in the software as 2 separate scan path linkers U100 spanning from Port 1 to Port 8 and U100_1 spanning from Port 9 to Port 16.

One scan path linker controls another

Where multiple scan path linkers are defined and one scan path linker controls another, for example, in Figure 21, a mother board controls a daughter board, you can set this up by nesting the OBL devices. In the software, drag an OBL device (DB Scan Path Linker) onto port 12 of the OBL device (MB Scan Path Linker) that will control it.

![Diagram](image-url)

Figure 21. Multi-core scan path linker (OBL Device) and nested scan path linkers.
Scan Path Linkers must not be part of individual chains

You must ensure that if an OBL device is being used as part of an individual chain, the OBL type cannot be changed until all chains which contain this device are deleted. Figure 22 shows the error message prompted when an OBL device that is part of a chain is deleted.

Automated Generation of ISL

The ISL to configure the scan path linker is generated after OBL chain creation is completed. Figure 23 is an example of the ISL that is generated in the Pre-Test section after the automated configuration of a scan path linker chain.
ISL for Lattice Devices

The following table details the ISL commands for Lattice devices.

<table>
<thead>
<tr>
<th>ISL Command</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABSCHAIN &quot;&lt;OBL_Dev1&quot;&gt;&quot;,&quot;&lt;OBL_Dev2&gt;&quot;;</td>
<td>Reference designator of OBL devices inserted in OBL_Dev1 and OBL_Dev2</td>
</tr>
<tr>
<td>ABSIR &quot;&lt;OBL_Dev1&gt;&quot; INST(SCANSEL), &quot;&lt;OBL_Dev2&gt;&quot; INST(SCANSEL);</td>
<td>Set the devices in Scan Select mode by instruction opcode SCANSEL</td>
</tr>
<tr>
<td>ABSDR &quot;&lt;OBL_Dev1&gt;&quot; DATA(16 bits hex data), &quot;&lt;OBL_Dev2&gt;&quot; DATA(16 bits hex data);</td>
<td>Select Register Mapping of the 16 bits of data is as below for Keysight x1149.</td>
</tr>
</tbody>
</table>

Select Register Mapping of the 16 bits of data is as below for Keysight x1149.

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
<td>EN</td>
<td>MS</td>
</tr>
<tr>
<td>Port</td>
<td>LSP8</td>
<td>LSP7</td>
<td>LSP6</td>
<td>LSP5</td>
<td>LSP4</td>
<td>LSP3</td>
<td>LSP2</td>
<td>LSP1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Local Scan Port (LSP) Control in the Select Register

<table>
<thead>
<tr>
<th>EN</th>
<th>MS</th>
<th>TMS for each scan port</th>
<th>TDO for each scan port</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>High</td>
<td>Z</td>
<td>Each LSP TMS is held High and TDO is set to High-Z mode (Default value when port is inactive)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Low</td>
<td>Z</td>
<td>Each LSP TMS is held Low and TDO is set to High-Z mode</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>TMS</td>
<td>Active</td>
<td>Each LSP TMS is driven by the value of TMS signal from the JTAG header and TDO drives the serial TDO data to the local scan chain (EN=1 and MS=0 is the value when the port is active)</td>
</tr>
</tbody>
</table>

ABSCHAIN;
ISL for Lattice Devices (continued)

The following table details the ISL commands for ScanSta devices.

<table>
<thead>
<tr>
<th>ISL Commands</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABSTRST 10;</td>
<td>Apply 10 TRST</td>
</tr>
<tr>
<td>ABSIR &quot;&lt;OBL_Dev&gt;&quot; INST(EXTEST)</td>
<td>Selects the OBL Dev</td>
</tr>
<tr>
<td>ABSIR &quot;&lt;OBL_Dev&gt;&quot; INST(MODESEL0)</td>
<td>Instruct Mode Select Register 0 into active scan chain.</td>
</tr>
<tr>
<td>ABSDR &quot;&lt;OBL_Dev&gt;&quot; DATA(8 bit Mode Register 0 bit configuration)</td>
<td>Selects Ports 0,1,2,3,4</td>
</tr>
</tbody>
</table>

| Bit 3 | Set to 0 by default so that TCK is free running when local scan ports are in Parked-RTI, Parked-Pause-DR or Parked-Paused-IR state. |

Set to 1
1. The TCK for each LSP stops and is held low when LSP is parked. This feature can be used in power sensitive applications to reduce the power consumed by the boundary scan circuitry in parts of the system that are not being used for boundary scan operations.
2. When LSPn is in the Parked-TLR state, TCKn is stopped after 512 clock pulses have been received on TCK independent of the bit3 value. This ensures that a hierarchical system consisting of SCANSTA112s on the LSPs of other SCANSTA112s will be reset when the LSPs of the SCANSTA112s at the first level of the hierarchy is replaced in the Parked-TLR state.

Bit 4 is used to enable daisy chaining of all the active ports from TDI to TDO when UNPARKed.

Bit 7 of mode register 0 is a status bit for the TCK counter. Bit7 is set to 1 when the TCK counter is ON and has reached terminal count(zero). It is cleared (set to 0) when the counter is loaded following a CNTRSEL instruction. The power-on value for bit7 is 0.

| ABSIR "<OBL_Dev>" INST(MODESEL1) | Instruct Mode Select Register 1 into active scan chain. |
| ABSDR "<OBL_Dev>" DATA (8 bit Mode Register10 bit configuration) | Selects Ports 5,6,7 |

| Bit 4 | is used to enable daisy chaining of all the active ports from TDI to TDO when UNPARKed. |

| ABSIR "<OBL_Dev>" INST(UNPARK); | With UNPARK instruction, scan chain configuration is set as defined by Mode Register 0 and Mode Register 1 settings. It activates TCK to free running mode. |
| ABSIR "<OBL_Dev>" INST(BYPASS); | Selects BYPASS instruction |
ISL for JTX Devices

The following table details the ISL commands for Lattice devices.

<table>
<thead>
<tr>
<th>ISL Commands</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABSIR &quot;&lt;OBL_Dev&gt;&quot; INST(EXTEST)</td>
<td>Select the OBL Dev to EXTEST mode</td>
</tr>
<tr>
<td>ABSIR &quot;&lt;OBL_Dev&gt;&quot; INST(IDCODE)</td>
<td>Select the OBL Dev to IDCODE mode</td>
</tr>
<tr>
<td>ABSDR &quot;&lt;OBL_Dev&gt;&quot; DATA(FFFFFFFF)</td>
<td>Fix data command</td>
</tr>
<tr>
<td>ABSDR &quot;&lt;OBL_Dev&gt;&quot; DATA(&lt;IDCODE Value&gt;)</td>
<td>Set Device IDCODE value based on the respective JTX family shown in the table</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>JTX device type</th>
<th>IDCODE value (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>JT X05</td>
<td>0001936F</td>
</tr>
<tr>
<td>JT X07</td>
<td>0001B36F</td>
</tr>
<tr>
<td>JT X09</td>
<td>0001D36F</td>
</tr>
</tbody>
</table>

ABSIR "<OBL_Dev>" INST(MODESEL) | Select MODESEL Register

ABSDR "<OBL_Dev>" DATA(0003) | Select Ports 1, 2

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Port 9</td>
</tr>
</tbody>
</table>

7 6 5 4 3 2 1 0
Port 8 Port 7 Port 6 Port 5 Port 4 Port 3 Port 2 Port 1

ABSIR "<OBL_Dev>" INST(UNPARK) | Select UNPARK Register

Note:
- JTX 09 supports 9 ports.
- JTX 07 supports 7 ports
- JTX 05 supports 5 ports
DFT for Scan Path Linker

When the project is set up as a scan path linker project, the DFT report after configuring the chain for the scan path linker is different. As shown in the report in Figure 24, the scan chain section describes the chain topology as per port specific topology for the scan path linker device (or OBL device) with port chains depicted respectively.

![DFT Report](image)

Figure 24: Scan path linker DFT report.

Benefits

This feature provides an automated mapping and configuration of local scan ports of the scan path linker (On Board Linker) device. It significantly reduces time and simplifies the process, when compared to the manual method of configuring scan path linker chains. The automated feature also facilitates configuration of nested scan path linkers across multiple boards (combo JTAG) easily. Details of the individual chain spanning across local scan ports of the scan path linker device, with active ports highlighted, are presented in the DFT report.

Conclusion

When a board has many devices involving several logic levels, the use of a scan path linker is recommended. This would reduce the real estate usage for boundary scan implementation and provide better management of a boundary scan chain. The automated scan path linker configuration feature on the Keysight x1149 compliments these designs by simplifying the project development, resulting in improved testing efficiency.
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