APPLICATION NOTE

IEEE 1687 – Silicon Test to Board Test

Why 1687?

Increasing demand for smaller and slimmer portable products with conscious focus to reduce power consumption is propelling more and more silicon Integrated Circuits (ICs) into squeezing multiple silicon dies or IPs (Intellectual Property) into a single IC package. To achieve this, in early 2000s semiconductor companies started packaging two-dimensional integrated circuit (2D IC) as Multiple Chip Modules (MCMs). Over the recent years, IC packaging has advanced into stacking different functional dies as a three-dimensional integrated circuit (3D IC). To this, the need for storing and processing more data has resulted into stacking multiple memory modules inside the IC package. Nowadays, performance centric applications like graphics use High Bandwidth Memory (HBM) into 3D for accelerating data access with lesser power consumption. All of this is a complex system residing in a Single IC package.

Reduce ASIC NTF

At-speed test to detect structural marginality

Detect Early-life failure of the silicon

With no access to the internals of such complex ICs, verifying that the logic circuits of these ICs are behaving correctly is a mind-boggling challenge. In addition to the logic test, getting access to, and testing the IPs embedded in these complex designs is even more important and challenging. Different IP usage from different vendors with differing complex test needs further exacerbates the challenge.

This in turn drives the need for standardization to access the IP and communicate the IP test needs, and processes to chip and system level test engineers. This is where IEEE 1687 standard evolved to formalize the access mechanism to the IP and its test procedures.

Growing Challenges for Test

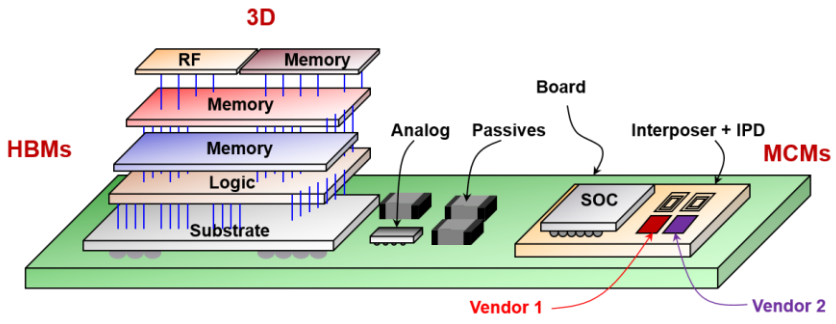

Figure 1: PCBA with Advanced Packaging and Multi-Chip Modules

KEYSIGHT TECHNOLOGIES

1687 Overview

The IEEE 1687 standard defines access mechanism for on-chip embedded instrumentation or IP (Intellectual Property) inside a chip. These embedded instruments are accessed via IEEE 1149.1 Test Access Port (TAP) specifically aimed at using the TAP to configure, operate and test on-chip embedded instruments. With the widespread use of embedded instrumentation for Built-In Self-Test (BIST) engine, complex I/O characterization and device calibration, IEEE 1687 finds prominence. IEEE 1687 fulfills standardization of access and management of the embedded instruments with an efficient and orderly process for the preparation of tests to access and control instruments, unlike custom implementations.

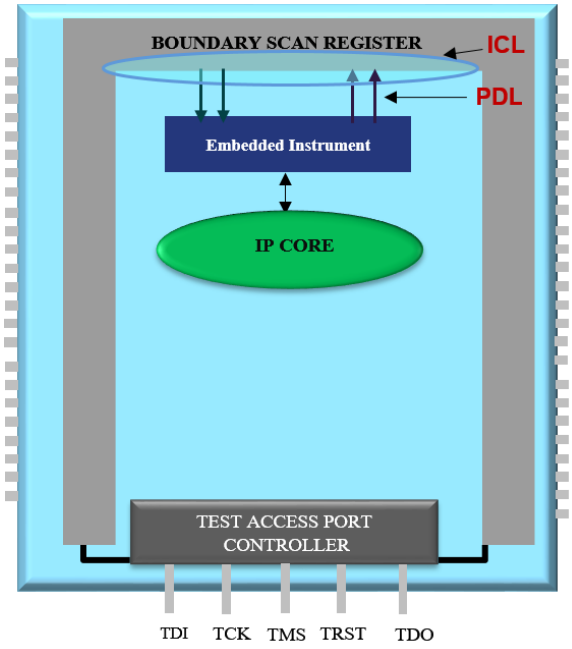

Figure 2: 1687 Overview

1687 Files

The IEEE 1687 standard defines two modelling languages – Instrument Connectivity Language (ICL) and Procedural Description Language (PDL).

Instrument Connectivity Language (ICL)

ICL describes the structure of the instrument access network that connects instruments to the device interfaces. This represents the elements like registers, etc. and logical connectivity from the JTAG interface of the chip - all the way through the Test Data Registers that interacts with the embedded instruments. ICL can be symbolically viewed as a BSDL file for the embedded IP. The chip IP designer delivers the ICL for the IP embedded instrument while the chip vendor delivers the ICL for accessing the IP from the chip's interface.

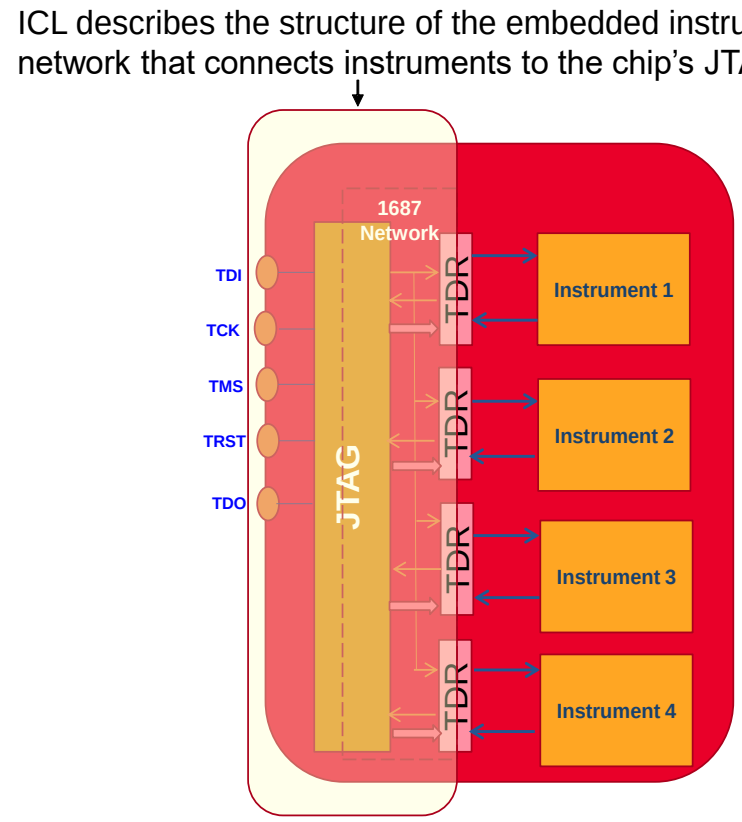

Figure 2: What does ICL describe?

Below is an example of a sample ICL file for an SPI instrument.

```
Module GPIO_IP {
  Attribute       IEEE1687_INSTRUMENT = "YES";
  ScanInPort     TDI                 { Attribute ALT_NAME="GPIO_TDI"; }
  ScanOutPort  TDO {
           Source tdr_GPIO[9];
  }
  ShiftEnPort      SHIFT_EN;
  CaptureEnPort    CAPTURE;
  UpdateEnPort     UPDATE;
  SelectPort       IP_SELECT;
  ResetPort        TRST;
  TCKPort          TCLK                { Attribute ALT_NAME="GPIO_TCLK"; }

  ClockPort        CLOCK;
  DataInPort       RESET               { Attribute REQUIRE_LO="YES"; }

  DataOutPort      IP_ACCESSED         { Attribute ALT_NAME="GPIO_IP_ACCESSED"; }

  ScanRegister     tdr_GPIO[9:0] {
         ScanInSource TDI;
  }

  ScanInterface GPIO_scan {
    Port TDI;
    Port TDO;
```

```
    Port IP_SELECT;
  }

}
```

PDL (Procedural Description Language)

PDL describes test procedures for testing an embedded instrument. The test procedures are described as sequences of stimuli and expected responses for the pins and registers are described in the ICL module for the instrument.

The chip IP designer delivers the PDL file for the corresponding IP. Typically, these are the test patterns that the IP designer has exercised to test the IP embedded in the chip. All this is packaged into a PDL file that can be streamed from chip, board or a system.

Some common PDL commands are:

iWrite – Specifies stimuli to the instrument

iRead – Specifies expected responses

iApply – Applies a group of iWrite and iRead commands to the IP

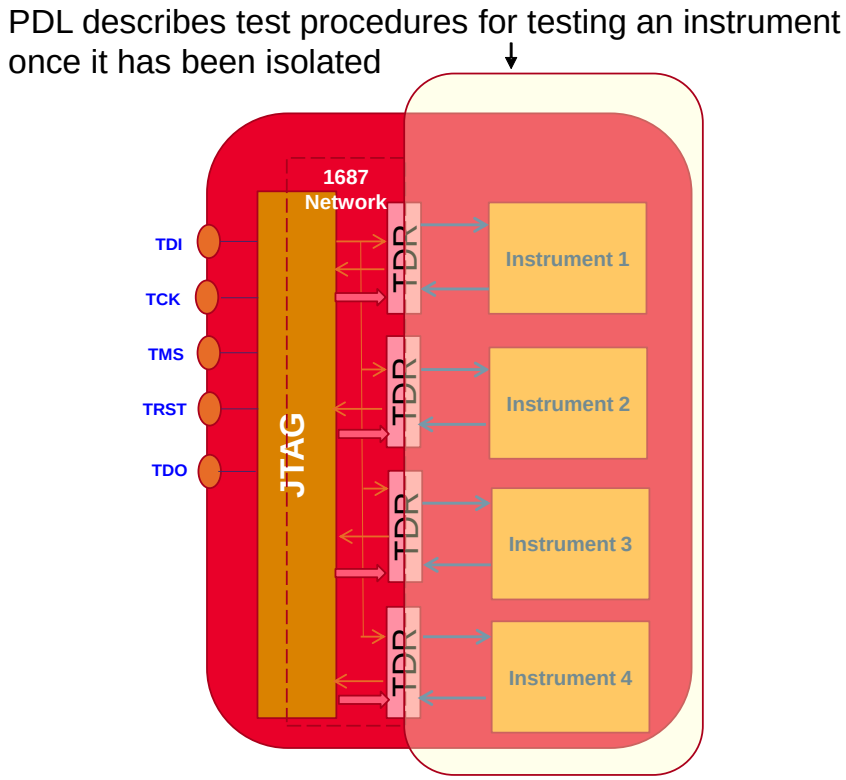

Figure 3: What does PDL describe?

Below is an example of a sample PDL file for a SPI instrument.

```
PDLLevel 0 -version STD_1687_2014;

iProcsForModule GPIO_IP;

iProc start_test {} {
   #iNote {#Select GPIO IP}
   iScan -ir GPIO_scan 8 -si 0xC8;

   #iNote {#Send LED pattern 10101010}

iWrite tdr_GPIO 0b1010101000;
iApply;
   iRead tdr_GPIO 0b10101010XX;
   iApply;

         #iNote {#Wait before sending the next set of patterns}
         iRunLoop 500;

   #iNote {#Send LED pattern 01010101}

   iWrite tdr_GPIO 0b0101010100;
   iApply;
   iRead tdr_GPIO 0b01010101XX;
   iApply;
}
```

IP Access with IEEE 1687

- ICL, like other hierarchical netlist description languages such as Verilog, uses the notions of “modules” and “instances” to define the relationship between the blocks in a design. Any time an instance statement is encountered, a parent-child relationship is established between modules that enables access from the top module all the way to instruments Test Data Registers. In the picture described above, ICL defines how an IP can be accessed from the chip top.
- PDL describes a structured flow of operations to be executed to test the IP.

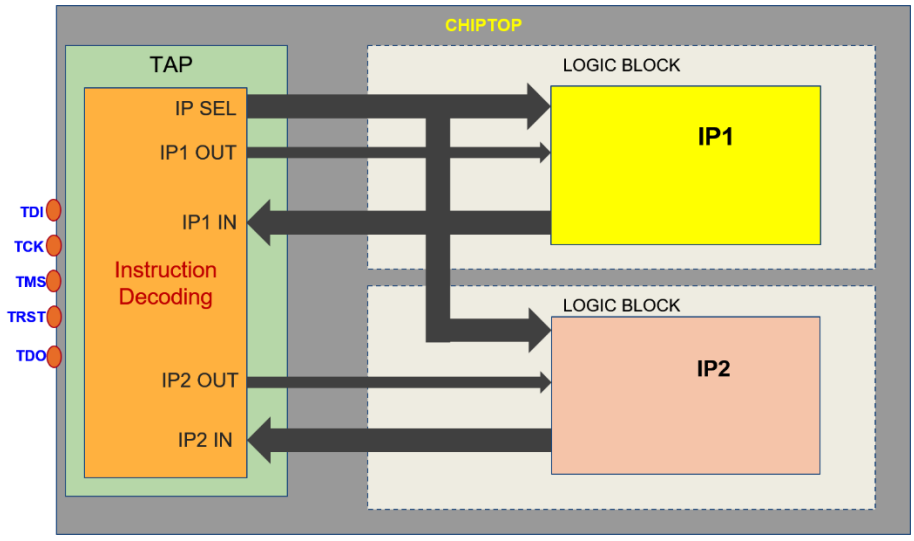

Figure 4: Chip Top with 2 1687 IPs

The relationship between modules (refer Figure 4) are hierarchically established across blocks from Chip Top Logic Bloc to IP via ICL definition. With ICL, the hierarchical access can be established in the link from Parent Block to Child block to Leaf block to Instrument to its TDR.

IEEE 1687 in Silicon Flow

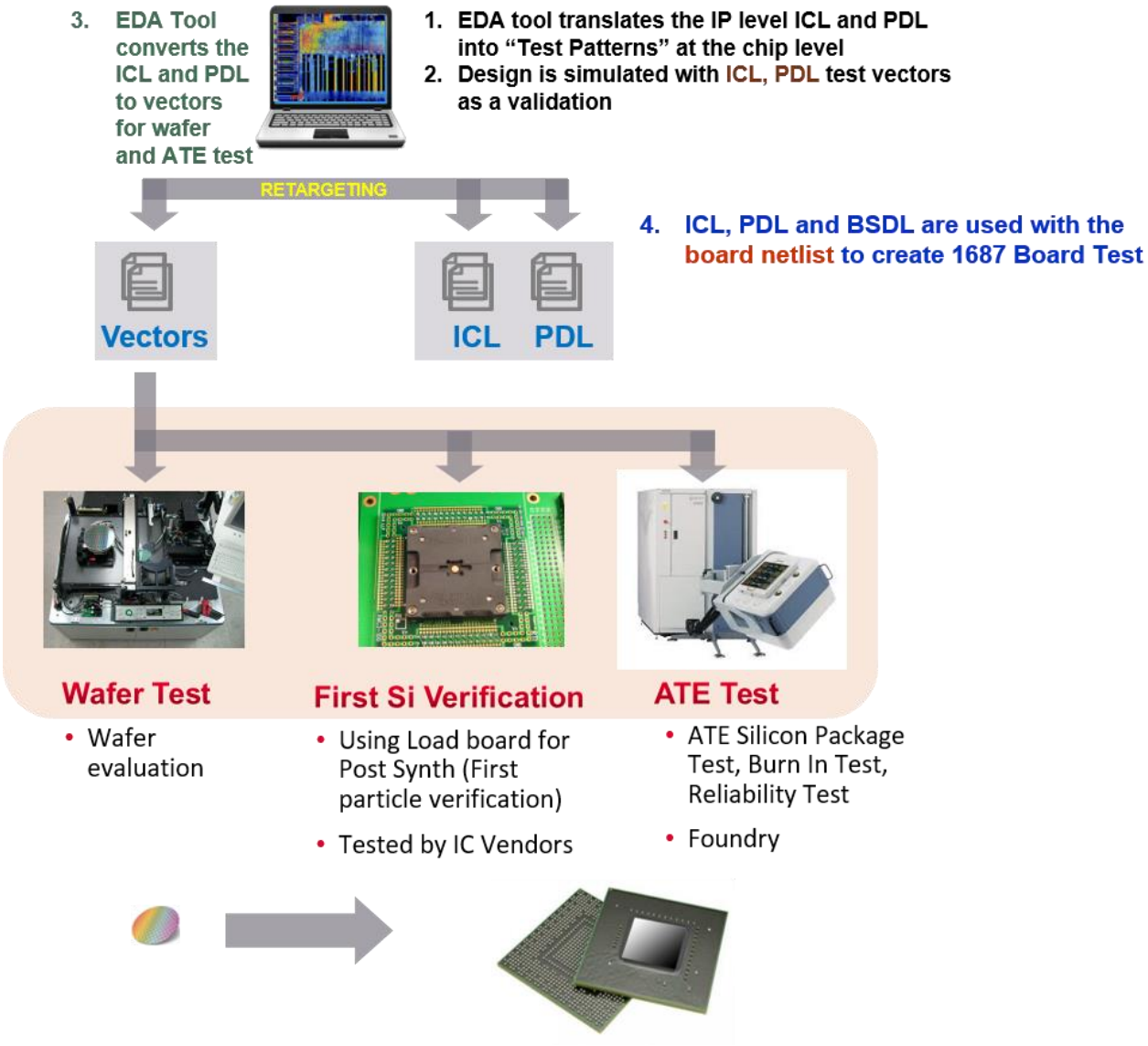

Figure 5: IEEE 1687 in Silicon Flow

Benefits of IEEE 1687 in Silicon Flow

1. Standardizes the mechanism to access and test IPs.
2. Simplifies testing of analog and mixed signal IPs.
3. Standardization eases 3rd party IP integration. and test Flexibility to integrate and test IPs as plug-n-play modules into System on Chip (SoC).

IEEE 1687 in Board Test Flow

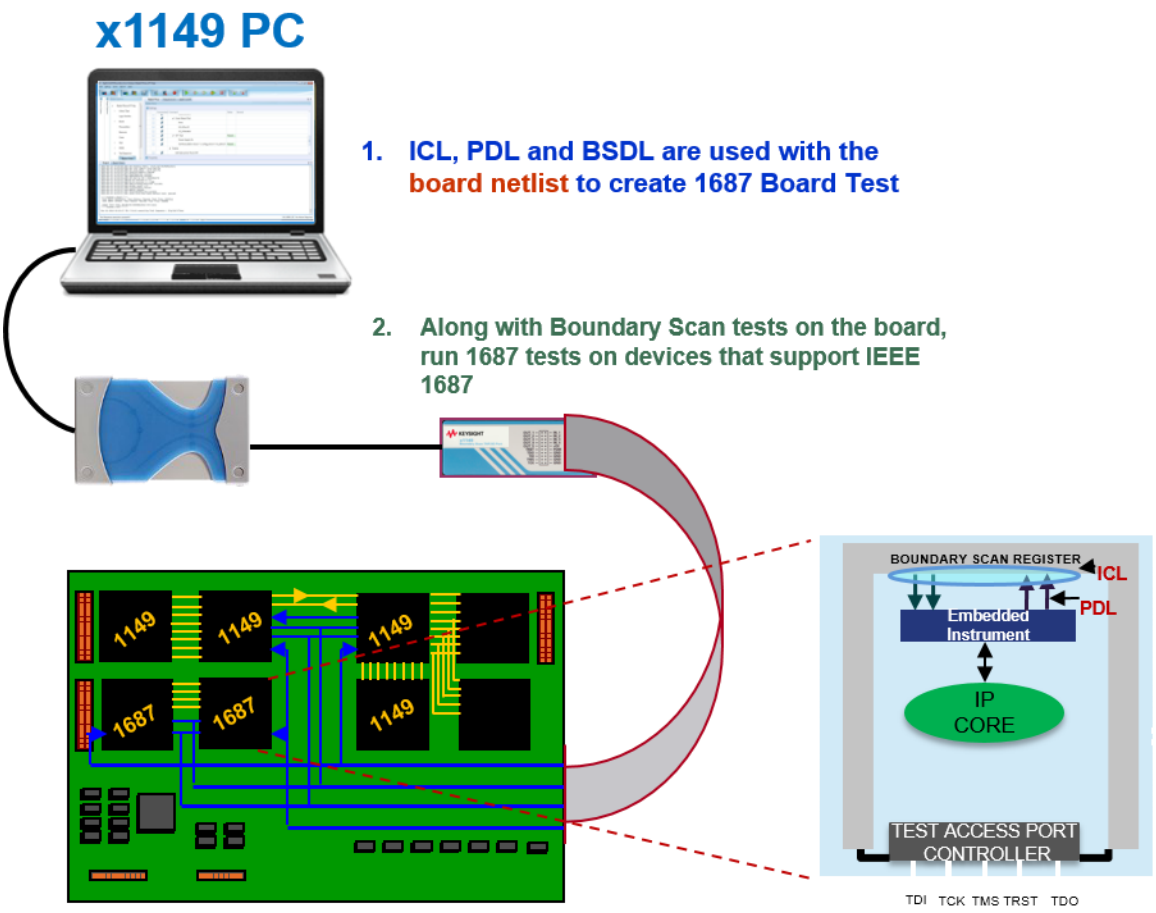

Figure 6: IEEE 1687 in Board Test Flow

Benefits of IEEE 1687 in Board Test Flow

1. Re-running structural tests on the same chip but in the new environment (on a board as opposed to on a chip tester) can reveal environmental dependencies (with power delivery, clock cleanliness, noise margins) that were not screened at the chip factory.

2. Re-running structural tests on the same chip later in the production flow can reveal early-life failure of the silicon, possibly caused by damage induced by the manufacturing process itself.

3. The structural test features (and some of the test content) of the components can be combined in new ways at the higher levels of integration to perform tests on the newly assembled subsystem that could never be applied until that point (for example, a Bit Error Rate Test from the transmitting chip through the actual channel on the board/backplane to the receiving chip).

Conclusion

We find that IEEE 1687 offers value from Silicon test until board test. It standardizes the mechanism to access and test IPs. These tests can be used for IP verification, wafer evaluation and, when integrated into top level IC package, these vectors can be leveraged for silicon verification. These tests can be run on the ATE (Automatic Test Equipment).

On the board, IEEE 1687 tests helps in reducing ASIC NTF (No Trouble Found) by detecting component issues early and by eliminating gross component failures before going to functional test. This helps in detecting early-life failure of the silicon - possibly caused by damage induced by the manufacturing process itself. With the component tests re-used from IP level until board level, it is effective in correlating the failures across different phases of the components lifecycle which ensures faster convergence on the root cause of the issues.