APPLICATION NOTE

4 Tools Simplify Boundary Scan Test Development And Debug On i1000D In-Circuit Test System

Improve Boundary Scan Debugging Efficiency

Introduction

Boundary Scan test technology (IEEE 1149) is now commonly used in the electronic test industry today.

In this document, we talk about four tools available on the Keysight i1000 In-Circuit Test (ICT) System that are essential to your boundary scan test development and debugging toolkit. Read on to learn more about these simple to use tools.

Boundary scan debugging tools:

- Handling large ICs with many pins
- Handling long interconnect tests
- Waveform Debugger
- Validating boundary scan tests using BST GUI

KEYSIGHT TECHNOLOGIES

1. Handling Large ICs With Many Pins

Testing many pins at the same time in a boundary scan test can result in Ground bounce. This phenomenon happens when many signals switch at the same time causing a reflection on the ground plane resulting in a “bounce” or oscillation on the ground connections. A common reason for ground bounce is because of an insufficiently low ground impedance in the PCB design. The result is a hang state in the logic gates in the device because the ground bounce puts the input of a flip flop effectively at voltage level that is neither a one nor a zero at clock time or causes untoward effects in the clock itself.

At the tester, one method to reduce the occurrence of ground bounce is to reduce the number of pins that are being tested at the same time. This reduces the number of signals that could toggle at the same and thus reducing the likelihood of ground bounce occurring.

The Keysight i1000D software includes a Connection Unit Size setting for boundary scan Interconnect and Connect test units that allows the test engineer to set the number of “connections” to be active for each “unit” of test.

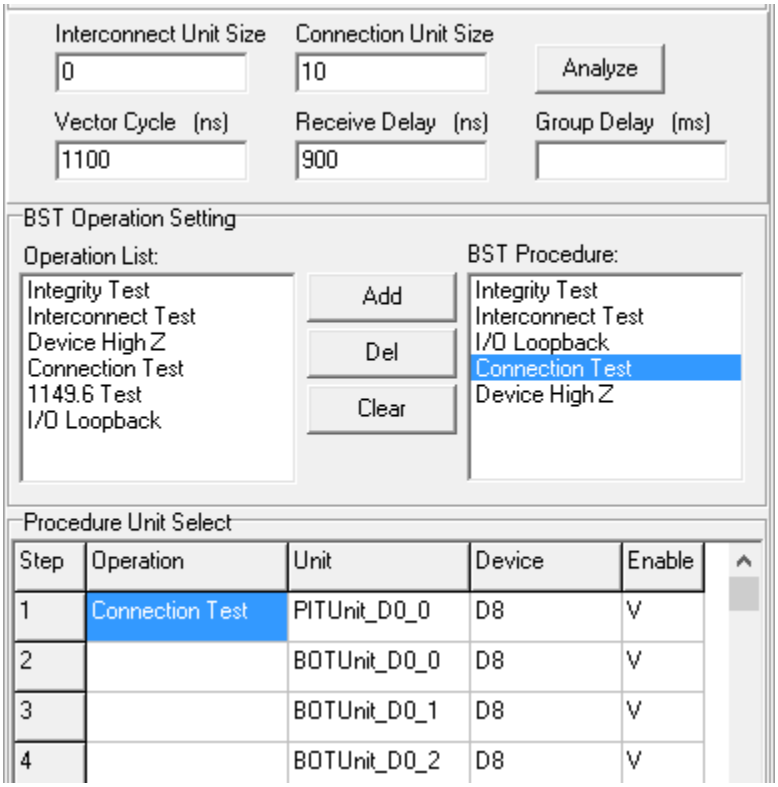

Figure 1-1: Connection Test List

For example, with the Connection Unit Size set to 10, after clicking the Analyze button the i1000D software will analyze the boundary scan test and allocate a maximum of 10 pins to each unit. Users will see multiple test units (POT, PIT, BOT or BIT) generated. Double clicking on each of the units will reveal the list of pins tested within that unit on the Result Message window on the right.

In cases where test engineer needs to disable the test on a specific pin on the boundary scan device, the i1000D software provides an easy and simple method. Given the example in Figure 1-3, the test engineer wants to disable pin K33 of U19 (U19.K33).

Click on U19 on the Device Configuration section to select it, then click on “Model Info.” button to view detailed information.

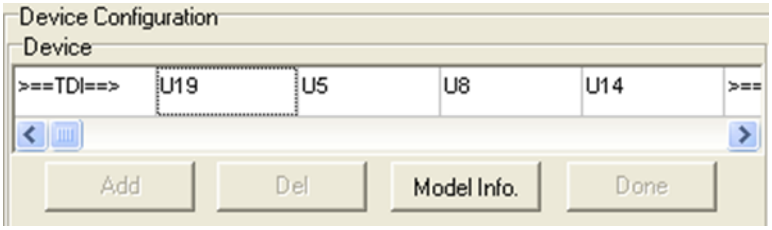

Figure 1-2: Model Information

The Model Information window opens and the BSDL file is loaded and displayed. Press Ctrl+F to search for pin K33 nail number. Once found, click Skip field on the 1st column of pin K33 to disable it from the test. In this way, the software will no longer include pin K33 in the boundary scan test.

404		403	BC_2	PLB_CS_N_2	output3	x	398	1	z	K32	out	10	0
405		404	BC_7	PLB_CS_N_1	bidir	x	398	1	z	L30	inout	10	0
406	V	405	BC_2	PLB_CS_N_0	output3	x	398	1	z	K33	out	10	5178

Figure 1-3: Commented One Node

For bidirectional cell which is defined as BIDIR function in the BSDL file, test engineer can select “test all”, “skip input”, “skip output” or “skip all” status.

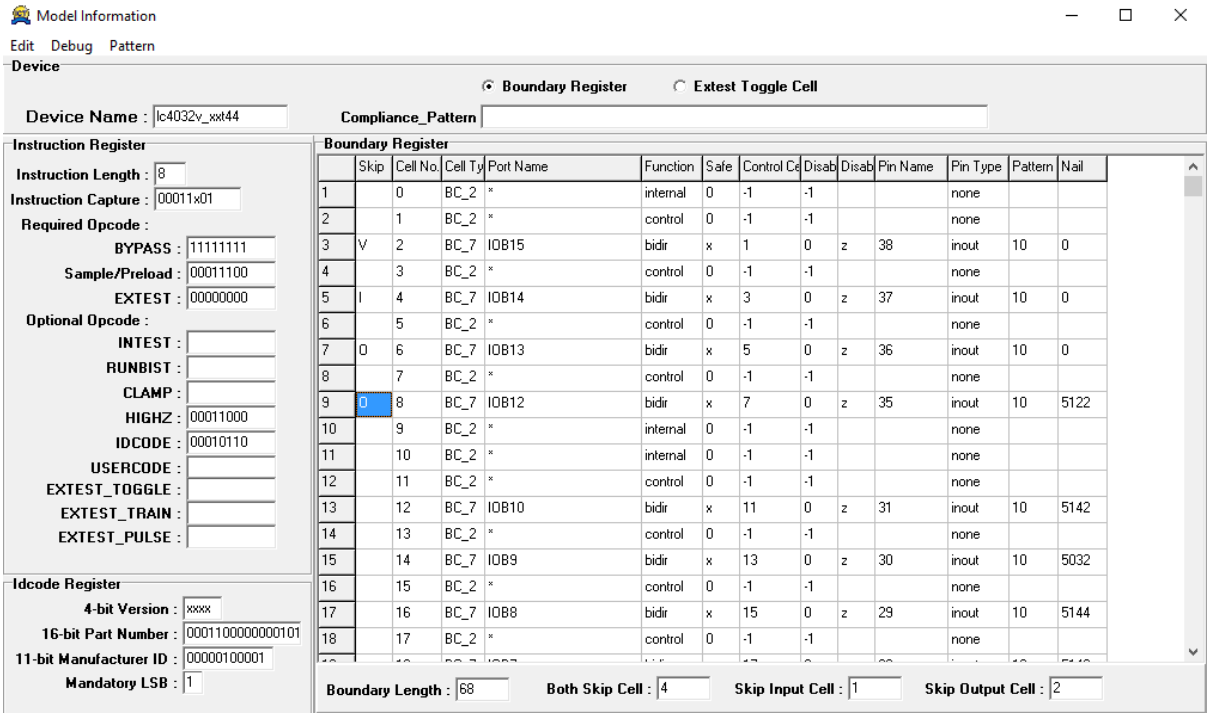

Figure 1-4: Skip One Status for Bidirectional Cell

In the window above, the test engineer can double click the “Skip” cell on the BIDIR function cell row to cycle through the different test modes. By default, it is blank. After double clicking the field, the letter “V” appears. The “V” means do not test this boundary cell. On the second double clicking of the field, the letter “I” appears. This means do not test input function for this bidirectional cell. On the third double clicking of the field, the letter “O” appears. This means do not test output function for this bidirectional cell. On the fourth double clicking of the field, it turns back to blank.

After modifying the test status, the Model Information window is closed, the software will prompt the test engineer to confirm settings. Click Yes to confirm settings.

The way to use these tools is firstly to set the maximum number of pins toggled within each test unit when developing the test. Then, if there is ground bounce issue seen, the test engineer can reduce the Connection Unit Size again or disable the pins individually in the test to understand the best number of pins to set. The Connection Unit Size is then reset, and the process is repeated to find the most optimum number of pins in each unit of test.

2. Handling Long Interconnect Tests

The Boundary Scan Interconnect test checks interconnect nodes between two boundary scan devices for opens and shorts, as shown in the figure below.

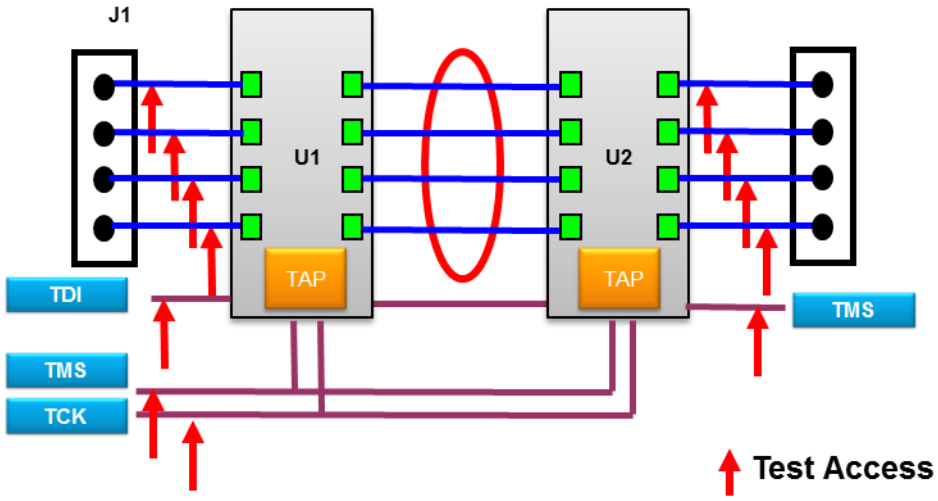

Figure 1-5: Interconnect Circuit

In order to reduce ground bounce issues, the i1000D software allows test engineers to select the maximum number of pins toggled within a test unit. The default setting is 0, meaning all the nodes are tested in one ITVUnit (Interconnect Test Unit). When the Interconnect Unit Size set to 10, for example, clicking on the Analyze button will cause the software to analyze the boundary scan test and allocate a maximum of 10 pins to each test unit.

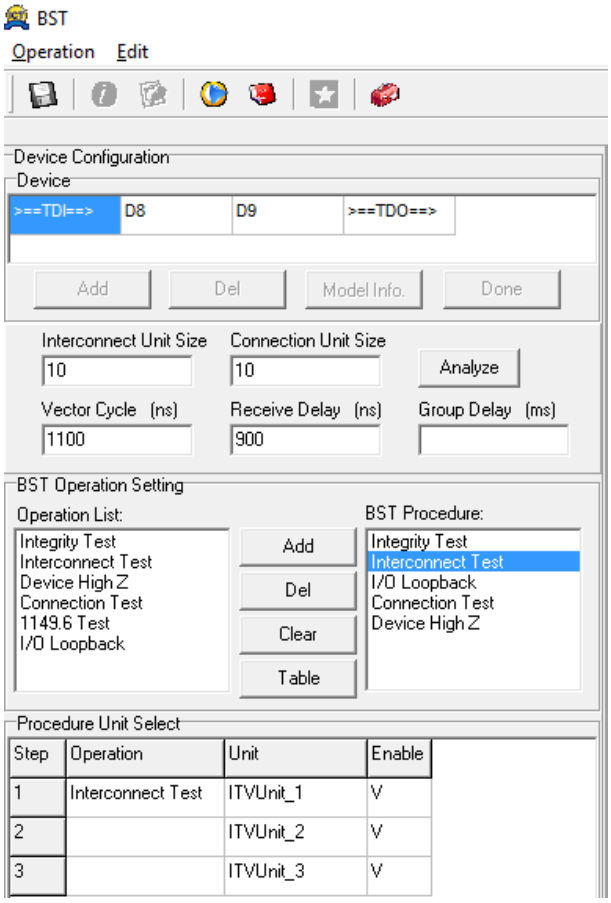

Figure 1-6: Interconnect Test List

When test engineer double clicks each ITVUnit, the Result Message window on the right of GUI will show information about the nets tested in the selected Interconnect test unit.

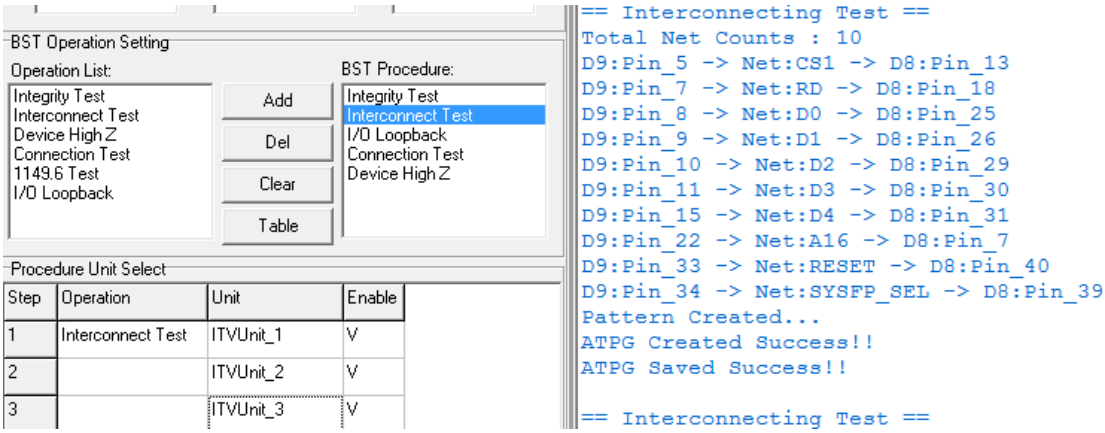

Figure 1-7: Test Nodes of Interconnect Test Unit

When the Table button is clicked, a spreadsheet will open. If user wants to skip any Net test, double click the first field of the row where the net resides. The “V” means this Net is skipped and will not be tested.

In one boundary scan chain, if both ends of bus has bidirectional cell, then the i1000 software will automatically generate a two-way boundary scan interconnect test for these cells.

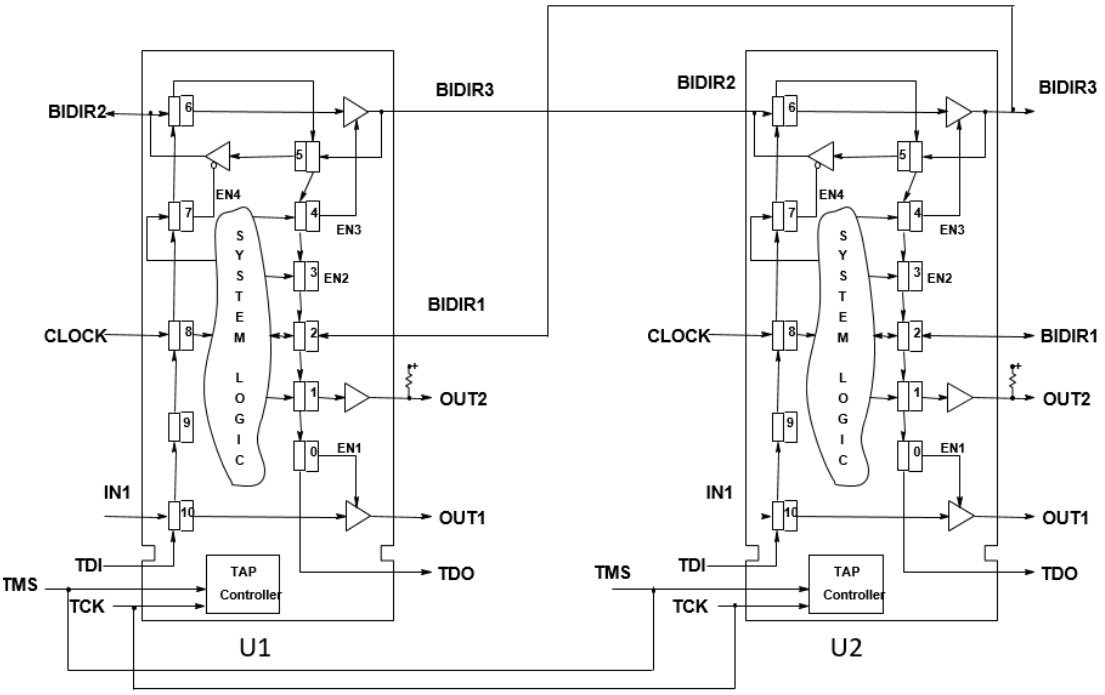

Figure 1-8: Interconnect of Bidirectional Cell

As shown in the diagram above, U1.BIDIR3 connects to U2.BIDIR2, and U1.BIDIR1 connects to U2.BIDIR3. The i1000 software will detect the connections based on BSDL file and generate two-way interconnect test.

As shown in the sample below, some signals generated two-way interconnect tests. The first two steps are tested and have the DONE signal. The first step is D8 drive to D9, and the second step is D9 drive to D8. Users can keep the two-way interconnect test or skip the one-way interconnect test like D3 and D2 signals.

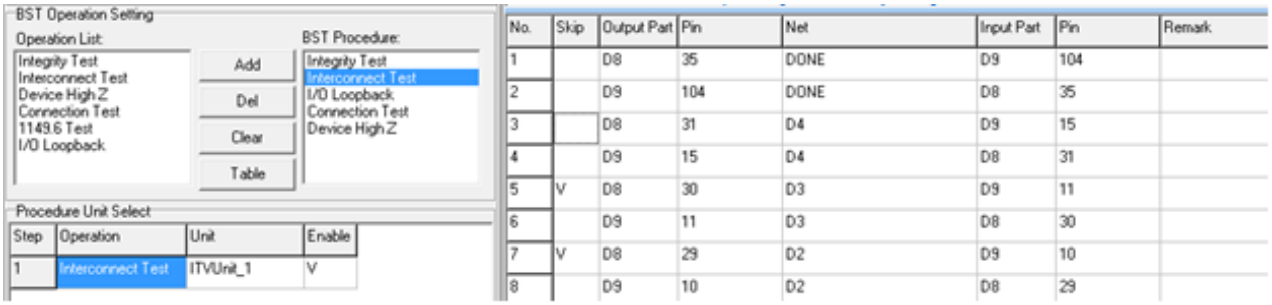

Figure 1-9: Commented Nodes in the Interconnect Test

Suggestion: For interconnect test debugging, test engineer can use mass edit function to set a block and skip the great mass of Nets, just keep one Net to be tested. After this Net test passed, un-skip other Nets, and try to test. So, follow this action to enable all of Nets.

3. Waveform Debugger

Debugging any boundary scans should start from its Integrity test. This ensures that the basic connections of the Boundary scan signals (TAP pins) is correct and that the Device ID of the physical part matched what is stated in the BSDL file.

Double click on Integrity Test under the BST Procedure section to have the software generates the test patterns internally. Then click on the Debug GUI icon  as shown below.

Figure 1-10: BST GUI Button

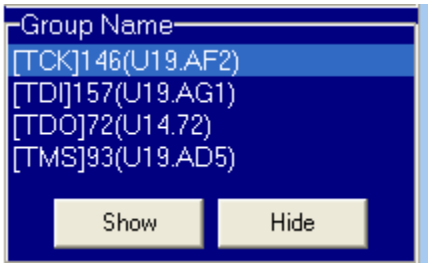

Figure 1-11: BST Group

On the bottom left of the Debug GUI, the Group Name section will list out the different signals used in that test. Simply double click on the signal name or click on Show button to display the selected signal on the graphic display.

The Debug GUI for boundary scan test allows test engineer to adjust the logic levels of each of the signal pins in the selected test. To adjust any signal, the selected signal must be displayed on the graphical window first.

When adjusting the logic levels, for example TDO, click to select the TDO signal on the graphic window and enter the required logic level in the provided fields on the left in the Logic Family section.

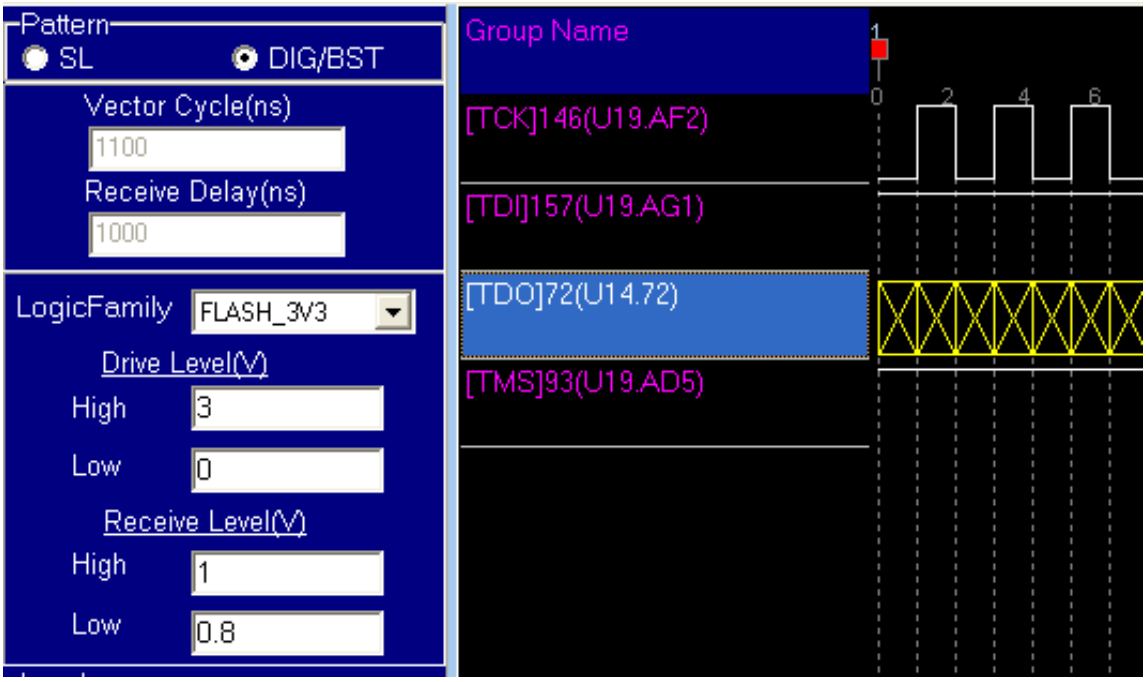

Figure 1-12: Logic Level Adjustment

After adjustment, click on the Save button located at the bottom right of the window and the test patterns will be updated immediately. Compilation or reload is not required.

Note: Any adjustments to the test will be saved into .sl file which is called supplemental library.

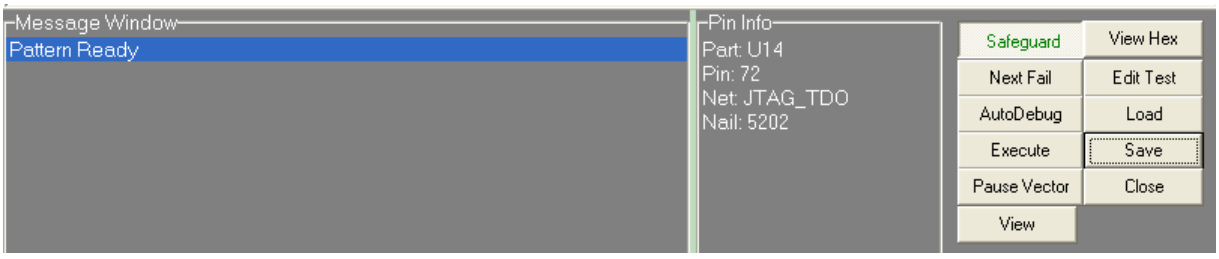

Figure 1-13: Message Window

The Message Window will show “Pattern Ready” which indicates that the test patterns are ready. Test engineer may now click on “Execute” button to run the test with the new settings.

On the waveform window, users can click any stage name at the bottom of the window, and the stage will be shown in the below table. As shown in the below sample, the current test execution stage is Shift-IR, the previous stage is Capture-IR.

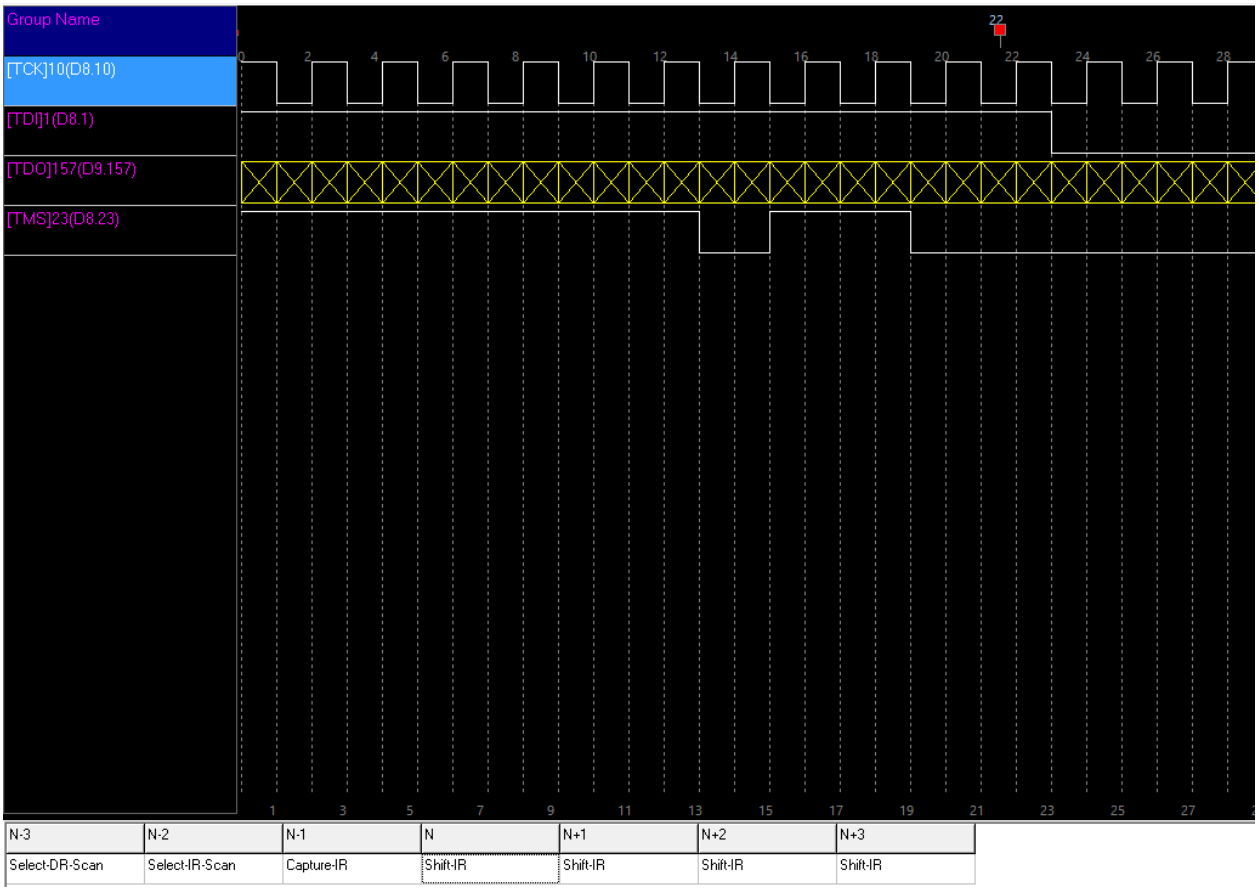

Figure 1-14: Waveform of Current Status

The Waveform Debugger allows the test engineer to easily view the boundary scan test vectors, understand what stage the test is in, adjust the logic family and logic levels. Use this tool to quickly debug your boundary scan test.

4. Validating boundary scan tests using BST GUI

After debugging every boundary scan test, users can run all selected boundary scan test in the i1000D BST GUI to verify them.

Click Run button to execute all the tests listed under the BST Procedure section. The test result will be shown at the top right corner of the window. If all tests passed, it will show a green “Pass” indicator. If a test failed, it will show a red “Fail” indicator.

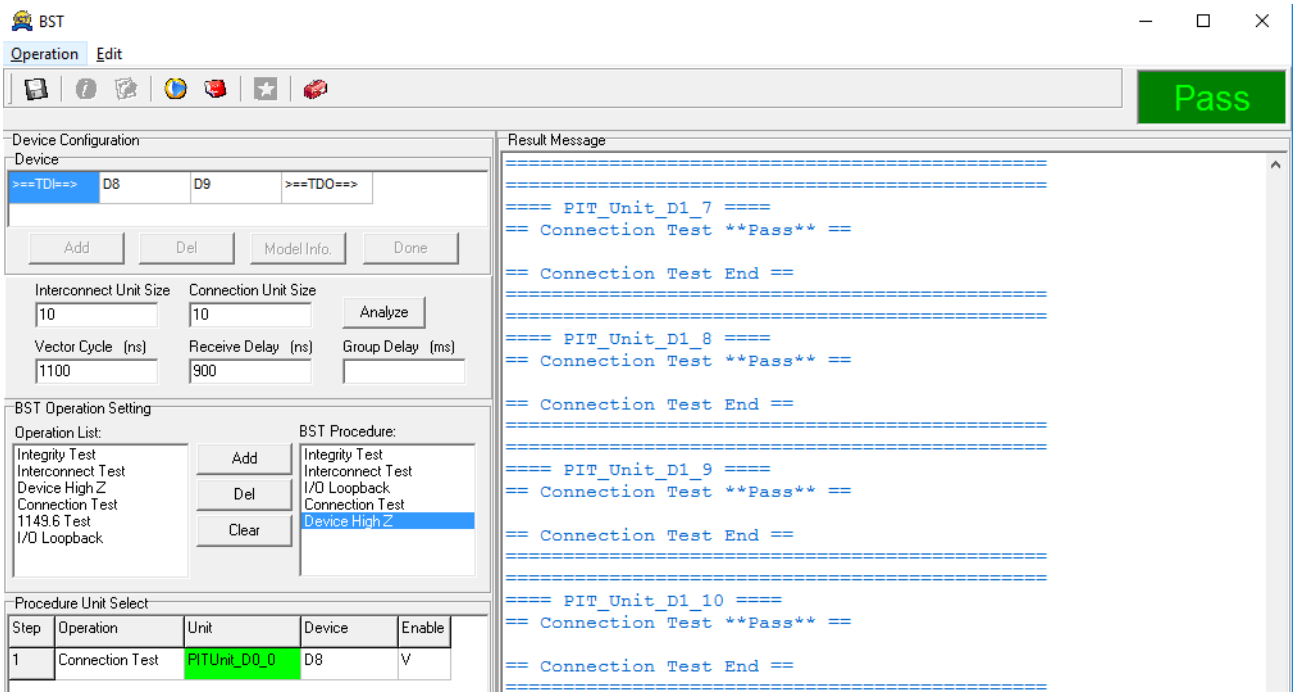

Figure 1-15: PASS/FAIL Information

Conclusion

The four tools described above are essential for developing and debugging boundary scan tests on the Keysight i1000D In-Circuit Test System. Using these tools will help you to build stable boundary scan test, quickly debug the test visually and easily validate all the boundary scan tests. Familiarize yourself with these tools to increase your efficiency in developing and debugging boundary scan tests on the i1000D ICT.

Web Resources

Keysight i1000 In-Circuit Test System: www.keysight.com/find/i1000

Keysight In-Circuit Test Systems: www.keysight.com/find/ict

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

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