APPLICATION NOTE

Requirement for Successful Boundary Scan Test Development on i1000D In-Circuit Test System

Reduce your engineering effort by following step by step implementation

Introduction

Boundary Scan test technology (IEEE 1149) is now commonly used in the electronic test industry today.

In this document, will talk about what test engineers should prepare to ensure good boundary scan implementation in order to reduce your engineering effort. The suggestions below are based on implementing boundary scan test on many different PCBAs of different functions over different i1000 In-Circuit Test (ICT) systems in different manufacturing sites across the world.

Requirements for success boundary scan implementation

- i1000D test fixture
- Stable DUT power on voltages
- Accurate BSDL file
- Correct driver / receiver logic levels

KEYSIGHT TECHNOLOGIES

Developing a boundary scan test

Boundary Scan test is no different from developing a digital test at ICT. All digital development and debugging tools can be used for boundary scan test development and debugging.

Just like developing a digital test, developing a good boundary scan test requires:

1) An i1000D test fixture with good digital signal quality
2) Stable working voltages on the DUT that is related to the Boundary Scan device
3) Accurate BSDL file
4) Correct Logic levels for the digital drivers/receivers.

1) A good i1000D fixture

Having an i1000D test fixture with good signal integrity is of the utmost importance. Over the years, one common question raised by ICT engineers is, “How can I debug my Boundary scan tests?” and my usual answer will be “Is the signal quality of your test fixtures good enough?”

In most cases, the common test engineer replies are:

“Of course, digital signal quality on my fixture is superb!”

“There’s no problem with my test fixtures”

“All the digital resources on my fixture has got ground plane isolation”

How can one verify the signal quality of the fixture? The best way is to probe the digital nodes on the fixture with an oscilloscope. Below is a screenshot showing the good quality TCK and TDO signals of a boundary scan test.

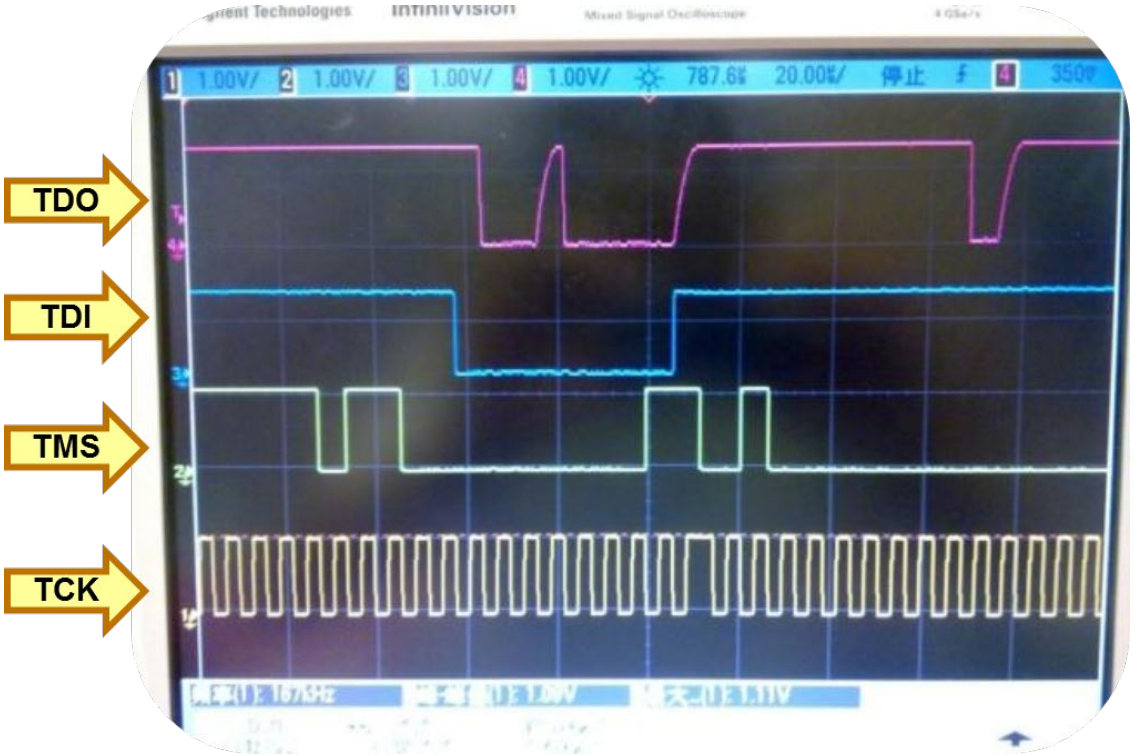

Figure 1-1: Actual Good Boundary Scan Signal

The engineers should look out for noise on the all the JTAG signals, especially on the TCK and TMS lines.

Noise sources could come from adjacent ICs, oscillators, sometimes from switching power circuits or from the fixture wiring.

The signal quality of short wires is better than long wires by reducing on crosstalk or impedance issues, therefore a good solution to remove noise is to reduce the fixture wire's length of the JTAG signals. In addition, the i1000 system is designed for excellent digital test signal integrity with a signal/ground ratio of 1:1 design, so it is easier to add twisted-pair wires in the fixture for all digital signals, thus shielding each signal wire from crosstalk.

The DUT board's DFT is also important. It is best to place all JTAG signals on the DUT board's bottom side, for shorter wires with similar wire lengths and impedance. If probes are placed on both sides of the DUT board, both the top and bottom fixture MUST be installed with ground-plants. The two ground plates MUST link up when the fixture is engaged. This will reduce the noise on the boundary scan signals and improve the signal quality.

2) Stable Working Voltage

Why do we need a stable working voltage especially to the Boundary scan device under test? Most test engineers will know the answer to this question. Without a stable working voltage, the device under test will not be operating in a stable condition and thus, any tests done will have unstable results.

Boundary scan devices may operate at several different input voltages. Voltages like +3.3V, +2.5V and +1.0V are common for large devices like micro-controllers and ASICs. Working with these devices will

need the test engineer to ensure that all its input voltages are available and stable throughout the entire boundary scan test sequence. Fluctuations to any of these input voltages can cause the device to go into an unknown state and stop responding to the boundary scan stimulus.

Nowadays, many board designers employ PWM (Pulse Width Modulation) as a method to control the power circuitry on their boards.

The PWM circuit converts an input reference voltage level to a pulse train of a specific pulse width in order to control the ON/OFF of power transistors or MOSFETs that output the required power to the power rails. A typical design starts with a triangular wave being fed into comparators. The comparators compare the triangular wave to a reference voltage and then switches its output accordingly, achieving a square wave with duty cycle controlled by the reference voltage. The higher the reference voltage, the longer the HIGH pulses on the square wave.

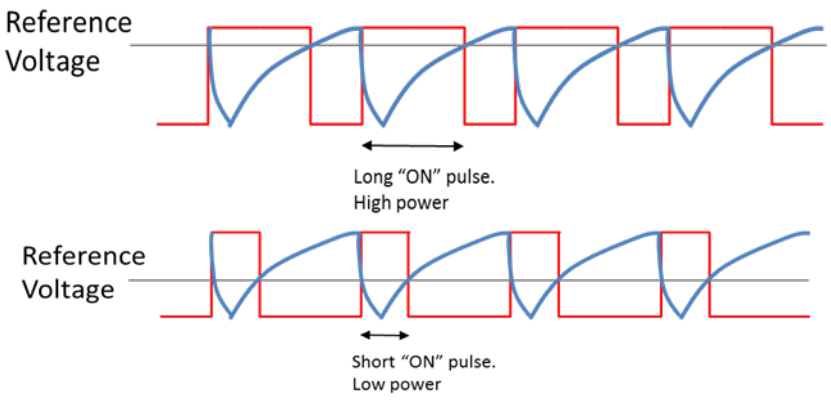

Figure 1-2: MOSFET ON/OFF Wave

The square wave is now used to control the ON/OFF state of the power transistors or FETs. Therefore, the higher the reference voltage, the longer the HIGH pulses and the longer the ON state. Controlling electrical power by means of quickly switching it on and off, and varying the "on" time, is known as Pulse-Width Modulation.

Combined with other sense and feedback circuitry, the PWM circuitry is a delicate and complex design. Any offset or interference to any part of the circuit may result in unstable output of the power supply or even totally turning off the power supply. This poses a huge challenge in In-Circuit Testing (ICT). Below is an example of a PWM circuit design.

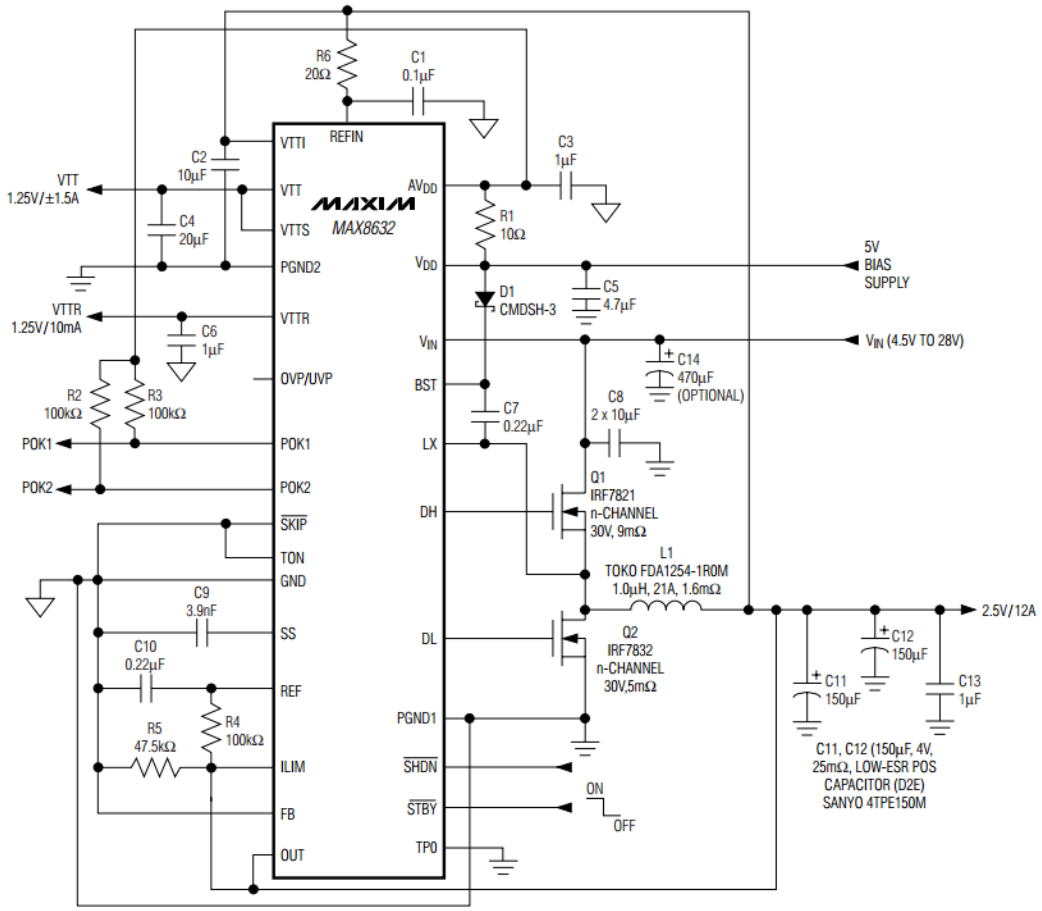

Figure 1-3: Typical PWM Circuit

On an ICT fixture, each probe on the fixture adds a certain amount of loading effect to testpoint on the board. These additional loads from the test probes may be just enough to cause the PWM to become unstable and affect its output. Therefore, it is recommended that all test probes around the PWM circuitry be removed leaving only the Input and Output probes. This clears all the sense and feedback signals of the PWM from the unwanted loads of the test probes and will help to ensure stability of the PWM operation.

But, is this enough? In most cases, isolating the PWM circuitry will directly result in much more stable working voltages. However, there are certain times where the power supplies are still interrupted during the Boundary scan test itself caused by the boundary scan test vectors themselves. If that happens, then detailed analysis of the boundary scan test signals and outputs will need to be conducted to see if there's any relation between the nodes involved in the Boundary scan test with the PWM circuit. If so, further isolation will need to be done.

During debugging of the boundary scan tests, it is recommended to insert tests to measure the voltage of the power rails before and after the Boundary scan test steps to help test engineers determine if the power voltages are correctly turned on during the test. These additional steps can simply be removed after debugging.

When the test fails intermittently, test engineers can monitor the boundary scan device's voltage using an oscilloscope during the test itself. Without stable working voltages, the boundary scan device will not operate stably.

3) Accuracy of BSDL file

The Medalist i1000D software can read a BSDL file without any need of editing its format. The software also checks and validates the contents of the BSDL file for syntactical errors and topological mismatches to the device when it is being assigned.

However, the i1000D software cannot determine if the file is the correct BSDL file for the targeted device on the board. There have been many cases when the revision of the BSDL file does not match the revision of the actual device assembled on the board. This is often seen during NPI stage when the designs are still fluid.

The test engineer needs to ensure that the BSDL for the right model and revision is used to develop the boundary scan test for that device assembled on the board. This will be the responsibility of the user. The test engineer needs to work with R&D engineers or sometimes with the IC manufacturer to ensure the validity of the selected BSDL. Only with the right BSDL, will you get the right results for the Boundary scan tests.

If the BSDL file is not accurate, unpredictable results will be seen during the debugging of the boundary scan test. Common BSDL errors found are related to wrong chain length, wrong boundary scan cell definition, wrong cell sequence or missing cells.

4) Logic levels of Digital drivers/Receivers

Regardless of the complexity of the digital test, selecting the correct logic family which matches the targeted device is crucial. Without defining the correct logic levels, the test can drive the digital test logics at the wrong voltage levels, thus, causing the device to be damaged.

How does a test engineer know what logic family to use for their Boundary scan device?

In most cases, test engineer can find the logic level information directly from the schematics. As shown in the example below, it can be easily seen that the boundary scan Test Access Port signals (TAP) uses the 3.3V logic. This is suggested by the pull up resistors (R171) on the TMS pin. Therefore, the logic family for TAP pins are programmed as below in the i1000D ICT:

Drive High = 3 to 3.3V
Drive Low = 0V
Receive High = 2 to 3V
Receive Low = 0.2 to 0.5V

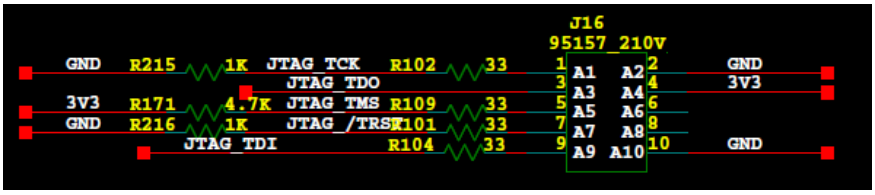

Figure 1-4: Sample of 3.3V Family

Similarly, in the next example, the TAP pins have pull high resistors to 2.5V. Therefore, the TAP pins are expected to operate in the 2.5V logic. Set the logic level as following:

Drive High = 2 to 2.5V
Drive Low = 0V
Receive High = 1 to 2V
Receive Low = 0.2 to 0.5V

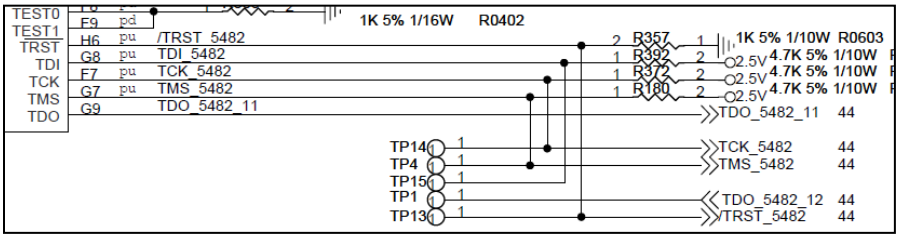

Figure 1-5: Sample of 2.5V Family

The next example shows that the TAP pins are not being pulled to any logic level. How is the logic family determined then?

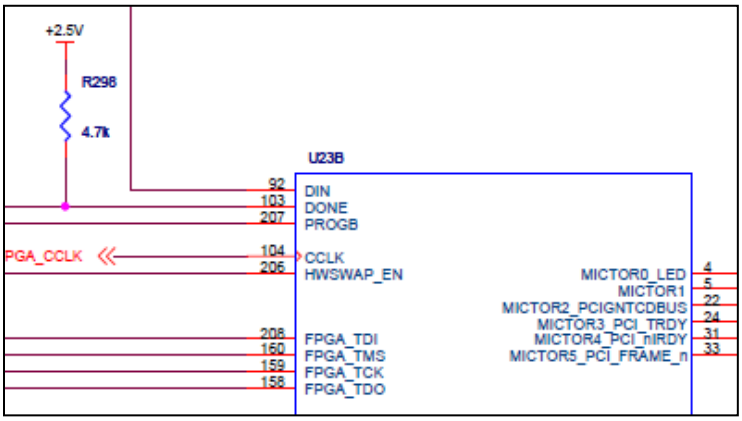

Figure 1-6: Sample of none pull up in the circuit

Usually, the logic levels of the TAP pins are the same as the operating voltage of the boundary scan device. Therefore, when the TAP pins do not contain any pull up information, referencing operating voltage of the device can help. Of course, there will still be cases where the TAP pins' logics level is different from the operating voltages. In this case, then it's down to a good understanding of the device's datasheet to get the correct logic level information for the device.

Conclusions

In most cases, with an accurate BSDL and correct logic level selection, the Integrity test can be easily turned on without problems. Good signal quality and stable working voltages are important for stable boundary scan tests, especially since there are usually thousands of digital vectors executed in boundary scan tests.

By ensuring the above 4 points will greatly improve the ease of implementation of the boundary scan test on the Keysight i1000 In-Circuit test system, thus reducing the test engineer's effort.

Web Resources

Keysight i1000 In-Circuit Test System: www.keysight.com/find/i1000

Keysight In-Circuit Test Systems: www.keysight.com/find/ict

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

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