Keysight M8000 Series of BER Test Solutions

J-BERT M8020A High-Performance BERT
M8030A Multi-Channel BERT
M8040A High-Performance BERT
Notices

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CAUTION

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A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.
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General
This product is a Safety Class 1 instrument (provided with a protective earth terminal). The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

All Light Emitting Diodes (LEDs) used in this product are Class 1 LEDs as per IEC 60825-1.

Environment Conditions
This instrument is intended for indoor use in an installation category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 95% and at altitudes of up to 2000 meters.

Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

Before Applying Power
Verify that all safety precautions are taken. The power cable inlet of the instrument serves as a device to disconnect from the mains in case of hazard. The instrument must be positioned so that the operator can easily access the power cable inlet. When the instrument is rack mounted the rack must be provided with an easily accessible mains switch.

Ground the Instrument
To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Do Not Operate in an Explosive Atmosphere
Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover
Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified personnel.

Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.
## Safety Symbols

### Table 1  Safety Symbol

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Symbol" /></td>
<td>Indicates warning or caution. If you see this symbol on a product, you must refer to the manuals for specific Warning or Caution information to avoid personal injury or damage to the product.</td>
</tr>
<tr>
<td><img src="image2" alt="Symbol" /></td>
<td>Frame or chassis ground terminal. Typically connects to the equipment's metal frame.</td>
</tr>
<tr>
<td><img src="image3" alt="Symbol" /></td>
<td>Indicates hazardous voltages and potential for electrical shock.</td>
</tr>
<tr>
<td><img src="image4" alt="Symbol" /></td>
<td>Indicates that antistatic precautions should be taken.</td>
</tr>
<tr>
<td><img src="image5" alt="Symbol" /></td>
<td>Indicates hot surface. Please do not touch.</td>
</tr>
<tr>
<td><img src="image6" alt="Symbol" /></td>
<td>Indicates laser radiation turned on.</td>
</tr>
<tr>
<td><img src="image7" alt="Symbol" /></td>
<td>CSA is the Canadian certification mark to demonstrate compliance with the Safety requirements.</td>
</tr>
<tr>
<td><img src="image8" alt="Symbol" /></td>
<td>CE compliance marking to the EU Safety and EMC Directives. ISM GRP-1A classification according to the international EMC standard. ICES/NMB-001 compliance marking to the Canadian EMC standard.</td>
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Compliance and Environmental Information

Table 2  Compliance and Environmental Information

<table>
<thead>
<tr>
<th>Safety Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>This product complies with WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste.</td>
</tr>
<tr>
<td></td>
<td>Product Category: With reference to the equipment types in WEEE Directive Annex I, this product is classed as a &quot;Monitoring and Control instrumentation&quot; product. Do not dispose in domestic household waste.</td>
</tr>
<tr>
<td></td>
<td>To return unwanted products, contact your local Keysight office, or see <a href="http://about.keysight.com/en/companyinfo/environment/takeback.shtml">http://about.keysight.com/en/companyinfo/environment/takeback.shtml</a> for more information.</td>
</tr>
</tbody>
</table>

Declaration of Conformity

Declarations of Conformity for this product and for the Keysight products may be downloaded from the Web. Go to http://www.keysight.com/go/conformity.

You can then search by product number to find the latest Declaration of Conformity.
About This Guide

Here is how the information in this document is organized.

Introduction
This chapter provides an overview of this manual.

Know Your Hardware
This chapter provides an information on the various modules of M8020A/M8030A/M8040A, their setup and the provided accessories.

Exploring M8070B User Interface
This chapter describes the M8070B user interface and the functionality provided by its common GUI elements.

Configuring Your System
This chapter describes how to configure the M8020A/M8030A/M8040A system using the Module View, Group View and System View.

Setting up Generator
This chapter provides information on settings provided by the M8020A/M8030A/M8040A Generator.

Setting up Analyzer
This chapter provides information on settings provided by the M8020A/M8030A/M8040A Analyzer.

Setting up Patterns
This chapter describes the functionality provided by the M8070B Pattern Editor and Sequence Editor.

Working with Measurements
This chapter describes the setup, execution, monitoring and results of the measurements supported by M8070B system software.

Utilities
This chapter describes the utilities provided by the M8070B system software.

Licenses
This chapter provides information on the M8020A/M8030A/M8040A and M8070B licenses and their installation procedure.

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This chapter provides information about basic troubleshooting and factory patterns.
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1 Introduction
Introduction

Overview

J-BERT M8020A high-performance BERT

The Keysight J-BERT M8020A high-performance BERT enables fast, accurate receiver characterization of single-and multi-lane devices running up to 16 or 32 Gb/s.

With today’s highest level of integration, the M8020A streamlines your test setup. In addition, automated in situ calibration of signal conditions ensures accurate and repeatable measurements.

Key Features

- Data rates up to 8.5 and 16 Gb/s expandable to 32 Gb/s
- 1 to 4 BERT channels in a 5-slot AXIe chassis
- Integrated and calibrated jitter injection: RJ, RJ1, RJ2, SJ, BUJ, sinusoidal level interference (common-mode and differential-mode), SSC (triangular and arbitrary, residual) and Clock/2
- 8 tap de-emphasis, positive and negative
- Integrated and adjustable Intersymbol Interference
- Interactive link training for PCI Express
- Built-in clock recovery and equalization
- All options and modules are upgradeable
M8020A Applications

The J-BERT M8020A is designed for R&D and test engineers who characterize and verify compliance of chips, devices, boards and systems with serial I/O ports up to 16 Gb/s and 32 Gb/s in the consumer, computer, mobile computing, data center and communications industry.

The J-BERT M8020A can be used to test popular serial bus standards, such as PCI Express®, SATA/SAS, DisplayPort, USB Super Speed, MIPI M-PHY, SD UHS-II, Fibre Channel, QPI, memory buses, backplanes, repeaters, active optical cables, Thunderbolt, 10/40 GbE/SFP+/QSFP, 100 GbE/CFP2.

M8030A Multi-Channel BERT

The M8030A Multi-Channel BERT extents the J-BERT M8020A platform to a real multi-channel BERT solution supporting up to 10 pattern generators and 10 error detectors (EDs) to allow multi-channel application tests like, PCIe and PON. Wherever multi-channel measurements are required in order to speed up throughput or test under real application conditions, the M8030A is a perfect solution.
1 Introduction

Key Features

- Data rates up to 8.5 and 16 Gb/s
- 1 to 10 BERT pattern generator and analyzer and channels in a 14-slot AXIe chassis
- Clock synchronization between all modules
- 8 tap de-emphasis, positive and negative
- Integrated and adjustable ISI
- Built-in clock recovery and equalization

M8030A Applications

The M8030A multi-channel BERT is designed for R&D and test engineers who characterize and verify compliance for electronic chips, devices, boards, systems with multiple I/O ports (up to 16 Gb/s) in various industry segments dealing with basic consumer goods, computer devices, communication equipments, etc. Typical applications are:

- PCIe multi-channel test
- PON applications
- XAUI and GAUI multi-lane test

M8040A High-Performance BERT

The Keysight Technologies M8040A is a highly integrated BERT for physical layer characterization and compliance testing.

With support for pulse amplitude modulation 4-level (PAM4) and non-return-to-zero (NRZ) signals, and symbol rates up to 64 Gbaud (corresponds to 112 Gbit/s) it covers all flavors of the emerging 400 GbE and CEI-56G standards.

The M8040A BERT’s true error analysis provides repeatable and accurate results, optimizing the performance margins of your devices.

Key Features

The M8040A provides the following features:

- Data rates from 2 to 32 and 64 Gbaud
- PAM4 and NRZ selectable from M8070B user interface
- Built-in 4 tap de-emphasis to compensate loss
- Integrated and calibrated jitter injection: RJ, RJ1, RJ2, SJ, BUJ, and Clk/2 Jitter
• Two pattern generator channels per module to emulate aggressor
• Linearity tests with adjustable PAM4 levels
• Short connections to the DUT with remote heads for the pattern generator
• True PAM4 error detection in real-time for low BER levels
• Graphical user interface and remote control via M8000 system software
• Scalable and upgradeable with options and modules
• Clock recovery with N1076A and N1077A

M8040A Applications

The M8040A is designed for R&D and test engineers who characterize chips, devices, transceiver modules and sub-components, boards and systems with serial I/O ports operating with data rates up to 32 Gbaud and 64 Gbaud in the data center and communications industries.

The M8040A can be used for receiver (input) testing for many popular interconnect standards, such as:
• 400 Gigabit Ethernet (IEEE 802.3bs)
• 200/100/50 Gigabit Ethernet
• OIF CEI - 56G (NRZ and PAM4 versions)
• 64G/112G Fibre Channel
• Infiniband-HDR
• CDAUI-8
• Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 Gbaud.
Document History

Table 3  Document History

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Related Documents

Table 4  Related Documents

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<tr>
<td>M8000-91B04</td>
<td>Tips for Preventing Damage</td>
</tr>
<tr>
<td>M8000-91B01</td>
<td>M8020A Start Here Document</td>
</tr>
<tr>
<td>M8000-91B02</td>
<td>M8030A Start Here Document</td>
</tr>
<tr>
<td>M8000-91B05</td>
<td>M8000 Series BER Test Solutions Installation Guide</td>
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<tr>
<td>M8000-91B06</td>
<td>M8020A/M8030A Getting Started Guide</td>
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<td>M8000 Series BER Test Solutions User Guide</td>
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<td>M8000-91B09</td>
<td>M8000 Series BER Test Solutions Programming Guide</td>
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<td>M8000 Series BER Test Solutions Plug-ins</td>
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<tr>
<td>M8000-91B10</td>
<td>M8000 Series Advance Measurement Package User Guide</td>
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<tr>
<td>M8000-91B11</td>
<td>M8000 Series Error Distribution Analysis Package User Guide</td>
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Abbreviations used in this Document

Table 5  Abbreviations

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<thead>
<tr>
<th>Abbreviation</th>
<th>Extended Form</th>
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<tr>
<td>AXIe</td>
<td>AdvancedTCA Extensions for Instrumentation and Test</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Extended Form</td>
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<tr>
<td>--------------</td>
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</tr>
<tr>
<td>AWG</td>
<td>Arbitrary Waveform Generator</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Ratio</td>
</tr>
<tr>
<td>CDR</td>
<td>Clock Data Recovery</td>
</tr>
<tr>
<td>CTLE</td>
<td>Continuous-Time Linear Equalizer</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>ESM</td>
<td>Embedded System Module</td>
</tr>
<tr>
<td>GB</td>
<td>Gigabyte</td>
</tr>
<tr>
<td>GUI</td>
<td>Graphical User Interface</td>
</tr>
<tr>
<td>J-BERT</td>
<td>Jitter-Bit Error Ratio Tester</td>
</tr>
<tr>
<td>LED</td>
<td>Light-Emitting Diode</td>
</tr>
<tr>
<td>MB</td>
<td>Megabyte</td>
</tr>
<tr>
<td>MIPI</td>
<td>Mobile Industry Processor Interface</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>PCIe</td>
<td>Peripheral Component Interconnect Express</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>PRBS</td>
<td>Pseudorandom Binary Sequence</td>
</tr>
<tr>
<td>PXI</td>
<td>PCI eXtensions for Instrumentation</td>
</tr>
<tr>
<td>R &amp; D</td>
<td>Research &amp; Development</td>
</tr>
<tr>
<td>SAS</td>
<td>Serial Attached SCSI</td>
</tr>
<tr>
<td>SATA</td>
<td>Serial Advanced Technology Attachment</td>
</tr>
<tr>
<td>SCPI</td>
<td>Standard Commands for Programmable Instruments</td>
</tr>
<tr>
<td>SMA</td>
<td>SubMiniature Version A</td>
</tr>
<tr>
<td>SSC</td>
<td>Spread Spectrum Clock</td>
</tr>
<tr>
<td>TCP</td>
<td>Transmission Control Protocol</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
</tbody>
</table>
2 Know Your Hardware

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M8020A Overview

The Keysight’s J-BERT M8020A High-Performance BERT is a modular instrument which supports the following modules:

- M8061A multiplexer 2:1 with de-emphasis 32 Gb/s.
- M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

In addition to above J-BERT modules, it also supports M8195A and M8196A Arbitrary Waveform Generator modules. Details of these modules can be found at www.keysight.com/find/m8195a and www.keysight.com/find/m8196a

M8020A being a modular product includes different sets of modules which are hosted in an AXI chassis. Each module and its features have their own license. You need to install these options in your instrument in order to use the modules or features. For details, refer to the chapter Licenses on page 547. However, if you have ordered M8020A-BU1, no license is required.

The M8041A module must be installed in slots 1 through 3 in the AXIe chassis unless the M9536A AXIe Embedded Controller is installed. The following configurations are possible in an M9505A 5-slot chassis:

- 1 or 2-channel, 16 Gb/s - (1) M8041A
- 3 or 4-channel, 16 Gb/s - (1) M8041A + (1) M8051A
- 1-channel, 32 Gb/s (Pattern Generator only) - (1) M8041A + (1) M8061A
- 1-channel, 32 Gb/s (Pattern Generator only or full BERT) - (1) M8041A + (1) M8062A
- M8195A/M8196A module can be added into the 5 slot module

Additionally, the M8061A, M8062A and M8195A/M8196A modules can be installed and operated in a 2 slot frame.

**NOTE**

In case an AWG module (M8195A/M8196A) is used in a combined system with M8020A modules, ensure that the AWG modules are mounted in a slot number higher than M8020A modules in the AXIe chassis. In other words, an AWG module always has to be mounted last in the chassis.
For details on the features and hardware components of each of the above-mentioned modules, refer to M8020A / M8030A Modules on page 38.

M9505A AXIe Chassis

The M9505A AXIe Chassis is a modular instrument chassis that supports complex and high density testing. The chassis provides slots for installing multiple AXIe based instrument modules such as the M8041A, M8051A, M8061A and M8062A modules. Besides providing a frame for the installation of these instrument modules, the M9505A AXIe Chassis also provides power, a cooling system, a PCIe Gen2 local data bus, a Gigabit LAN interconnect, and a cabled USB (USB option required) and PCIe connection for external host computer connectivity.

The following model of the M9505A AXIe Chassis supports the M8020A modules:
- M9505A - a 5-Slot AXIe chassis

**NOTE**

The USB connection is recommended when using a laptop or desktop PC as an external controller. The PCIe connection is recommended for use with a desktop PC as an external controller only.

Refer to the Keysight M9505A AXIe Chassis Startup Guide to get detailed information about the AXIe chassis.
AXIe Embedded System Module (USB ESM)

The bottom slot of the AXIe chassis is reserved for the Embedded System Module (ESM) which is factory-installed. The ESM has a USB 2.0 interface as well as a PCIe x8, Gen1 and Gen2 compliant interface to connect an external host computer to the chassis. The following figure shows the PCIe Port and USB Port in ESM.

The ESM:
- runs the chassis embedded operating system which manages all internal tasks and communications.
- tracks inserted modules and manages power requirements.
- monitors chassis temperature and controls variable-speed chassis fans.
- monitors module sensors and reports component failures to a system log.
- acts as a Gigabit Ethernet switch; forwards frames along the backplane.
- connects an external host computer to the chassis.
- synchronizes timing across all modules through the Keysight Trigger Bus, using an internal or external clock source.
- LAN connector on AXIe ESM is not used. Only use LAN connection on the host computer.
- Either the PCIe (desktop only) or USB (desktop or laptop) port can be used in this ESM but not both simultaneously. When you use the PCIe port, the USB port is automatically disabled until the PCIe port is no longer in use.
Host Computer

A host computer is used to:

- host all the software components of the instrument modules needed to control, configure, and use the modules.
- communicate with the ESM of the M9505A AXIe Chassis to allow you to monitor and control the chassis.

A host computer can be:

- the M9537A AXIe Embedded Controller module.
- a laptop with a USB port or with PCIe port.
- a desktop PC with a USB port or x8 or wider PCIe slot for the cabled PCIe adapter card.

Keysight M9537A AXIe Embedded Controller Module

The M9537A AXIe Embedded Controller is a one slot module that you can install in the M9505A AXIe Chassis like any other instrument module. This module acts as a host computer when installed in the M9505A AXIe Chassis. It is always installed in slot 1 of the M9505A AXIe Chassis.

The following figure displays this module.
M8030A Overview

The M8030A is a modular instrument which supports the following modules:

- M8041A high-performance BERT generator-analyzer-clock 8/16 Gb/s
- M8051A high-performance BERT generator-analyzer 8/16 Gb/s
- M8092A Multi-channel synchronization module

The modules must be installed in the M9514A AXIe 14-slot chassis in the following way:

<table>
<thead>
<tr>
<th>Slot Number</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td># 1</td>
<td>M8030A-BU1 AXIe embedded controller. For M8030A-BU2 this slot is empty and covered with filler front-plane</td>
</tr>
<tr>
<td># 2, 3 &amp; 4</td>
<td>M8041A module</td>
</tr>
<tr>
<td># 5 &amp; 6</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 7</td>
<td>M9521A AXIe system module, always included in M8030A-BU1 or M8030A-BU2, must be in this slot</td>
</tr>
<tr>
<td># 8 &amp; 9</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 10 &amp; 11</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 12 &amp; 13</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 14</td>
<td>M8192A multi-channel synchronization module, always required in this slot</td>
</tr>
</tbody>
</table>

For details on the features and hardware components of each of the above mentioned modules, refer to *M8020A and M8030A Getting Started Guide*. 
M9514A AXIe Chassis

The Keysight M9514A AXIe 14-slot chassis (one slot for the AXIe System Module plus 13 instrument module slots) is a modular instrument chassis fully compatible with the AXIe 1.0 Hardware specifications. It allows multiple application-specific instrument modules to share a common chassis frame, power supply, cooling system, PCI Express (PCIe) Gen 2 data bus, Gigabit LAN hub, local bus for module-to-module signaling, and host PC connections.

Multiple chassis may be interconnected for scalability. The chassis provides 13 general purpose peripheral slots that accept AXIe instrument modules. Each module slot has a Gen 2 x4 link (maximum of 2 GB/s data rate per module) to the chassis primary data ‘fabric’ hub—a x8 PCIe switch and data bus.

The chassis requires a full module height AXIe System Module (ASM) such as the Keysight M9521A, to manage chassis functions.

**NOTE**

The USB connection is recommended when using a laptop or desktop PC as an external controller. The PCIe connection is recommended for use with a desktop PC as an external controller only.

**NOTE**

PCIe connectivity between the M9514A AXIe Chassis and an external desktop PC controller is recommended when full channel plus large patterns need to be downloaded.

Refer to the Keysight M9514A AXIe Chassis Startup Guide to get detailed information about the AXIe chassis.
AXIe System Module (ASM)

The M9521A AXIe System Module (ASM) is installed in the system slot of the M9514A (slot 7). It provides the system communication and synchronization functions required in an AXIe chassis including:

- Trigger bus and clock routing.
- Managing clocks, including internal or external reference sources.
- Gigabit LAN switching with front panel RJ45 LAN connections.
- AXIe Fabric 1 switching (Gen 2 x4 lanes to each module slot).
Keysight M9537A AXIe Embedded Controller Module

The M9537A AXIe Embedded Controller is a one slot module that you can install in the M9505A/M9514A AXIe Chassis like any other instrument module. This module acts as a host computer when installed in the M9505A/M9514A AXIe Chassis. It is always installed in slot 1 of the M9505A AXIe Chassis. It may be installed in any slot of the M9514A AXIe chassis except for Slot 7 which is reserved for the ASM. However, to eliminate interference with the local bus used for E-Keying (if your AXIe modules use E-Keying), you should install the controller in one of the outside slots; e.g., 1 or 14 first, then 2 or 13, etc.

The following figure displays this module:

The ESM:
- runs the chassis embedded operating system which manages all internal tasks and communications.
- tracks inserted modules and manages power requirements.
- monitors chassis temperature and controls variable-speed chassis fans.
- monitors module sensors and reports component failures to a system log.
- acts as a Gigabit Ethernet switch; forwards frames along the backplane.
- connects an external host computer to the chassis.
- synchronizes timing across all modules through the Keysight Trigger Bus, using an internal or external clock source.

LAN connector on AXIe ESM is not used. Only use LAN connection on the host computer.

Either the PCIe (desktop only) or USB (desktop or laptop) port can be used in this ESM but not both simultaneously. When you use the PCIe port, the USB port is automatically disabled until the PCIe port is no longer in use.
M8020A / M8030A Modules

The M8020A/M8030A modules are recognized by the model number and name located on their front panel.

Each BERT module can be configured for 8 Gb/s or 16 Gb/s operation, as generator-only or as full BERT. Some upgraded features/components of a module are licensed and are only available when you purchase a license for that option. The M8062A module supports 32 Gb/s and the M8195A as a BERT module can support higher speeds than 16 Gb/s. The M8195A cannot be used as a full BERT. It has no analyzer.

The following sections describe each of the M8020A/M8030A instrument modules in detail.

J-BERT M8041A Generator-Analyzer-Clock Module

The J-BERT M8041A is a BERT module that can be installed into an Keysight M9505A 5-slot AXIe chassis. This module occupies three slots.

The M8041A is a two channel bit error ratio tester with built-in clock and data generator for performing compliance and characterization measurements. The second channel requires a license.

M8041A Features

The M8041A module provides the following features:

- Two channel pattern generator (option 0G2) and two channel error detector (option 0A2)
- Data rate from 256 Mb/s to 16.2 Gb/s (option G16 or C16) for pattern generation and error detection
- Built in jitter injection (option 0G3)
Know Your Hardware

- Adjustable ISI offered for M8041A and M8051A (option 0G5), software 2.0 and serial number >= DE55300500
- Built in 8 tap de-emphasis (option 0G4)
- Built in receiver equalization (CTLE, option 0A3)
- Built in reference clock multiplier for pattern generator (option 0G6)
- Simultaneous common mode and differential mode level interference (option 0G7)
- Interactive link training (option 0S1, Software 1.5)
- Four universal control inputs with adjustable threshold
- Three universal control outputs with adjustable levels
- 2 Gb pattern memory per channel (requires software 1.5)

**M8041A Module Components**

The following figure displays the front panel of the M8041A module with its various components labeled.
The M8041A module has the following components.

**Table 7  Insertion/Extraction and Retaining**

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Retaining screws</td>
<td>The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.</td>
</tr>
<tr>
<td>Module Insertion/Extraction Handles</td>
<td>The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.</td>
</tr>
</tbody>
</table>

**Table 8  Front Panel LEDs**

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Active when...</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fail</td>
<td>power-up fault condition</td>
<td>red</td>
</tr>
<tr>
<td>Access</td>
<td>power-up ready state</td>
<td>green</td>
</tr>
<tr>
<td>Data In x</td>
<td>input is overloaded</td>
<td>red</td>
</tr>
<tr>
<td>Data Out x</td>
<td>output is overloaded</td>
<td>red</td>
</tr>
<tr>
<td>Data Mod In x</td>
<td>input is active</td>
<td>green</td>
</tr>
<tr>
<td>Ctrl In A/Ctrl In B</td>
<td>logic level is detected</td>
<td>green</td>
</tr>
<tr>
<td>Ctrl Out A</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Clk In</td>
<td>signal is detected</td>
<td>green</td>
</tr>
<tr>
<td>Ref Clk In</td>
<td>signal is detected</td>
<td>green</td>
</tr>
<tr>
<td>Ref Clk Out</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Aux In</td>
<td>not used</td>
<td>n/a</td>
</tr>
<tr>
<td>Clk Out</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Trig Out</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Clk Mod In</td>
<td>input is active</td>
<td>green</td>
</tr>
<tr>
<td>Sys Out A/Sys Out B</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Sys Ctrl In A/Sys Ctrl In B</td>
<td>logic level is detected</td>
<td>green</td>
</tr>
</tbody>
</table>
The inputs of the M8041A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

### Table 9  Channel x Data Inputs/Outputs

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Out and /Data Out</td>
<td>Differential data outputs (3.5 mm, female).</td>
</tr>
<tr>
<td>Data In and /Data In</td>
<td>Differential data inputs (3.5 mm, female).</td>
</tr>
<tr>
<td>Data Mod In</td>
<td>Accepts an external source for data out delay modulation (SMA, female).</td>
</tr>
</tbody>
</table>

### Table 10  Clock Inputs/Outputs

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clk In</td>
<td>External clock input in the range of 8.1 to 16.2 GHz. This input is used as</td>
</tr>
<tr>
<td></td>
<td>a direct clock for all channels in forwarded clock applications (SMA, female).</td>
</tr>
<tr>
<td>Ref Clk In</td>
<td>Reference clock input for applications that provide a host reference clock</td>
</tr>
<tr>
<td></td>
<td>in the range of 10 MHz to 16 GHz. The clock signal may be SSC modulated and</td>
</tr>
<tr>
<td></td>
<td>is used as the reference for the system clock of all Tx and Rx channels. A</td>
</tr>
<tr>
<td></td>
<td>SSC tolerant PLL is used to multiply the reference clock to the system clock</td>
</tr>
<tr>
<td></td>
<td>(SMA, female).</td>
</tr>
<tr>
<td>Ref Clk Out</td>
<td>The reference clock output is used to provide a 10 MHz or 100 MHz reference</td>
</tr>
<tr>
<td></td>
<td>clock to the DUT or other test equipment (SMA, female).</td>
</tr>
<tr>
<td>Clk Out and /Clk Out</td>
<td>Differential clock output (3.5 mm, female).</td>
</tr>
<tr>
<td>Trig Out and /Trig Out</td>
<td>This output is used to send a trigger signal to another connected device,</td>
</tr>
<tr>
<td></td>
<td>such as an oscilloscope (3.5 mm, female). It can also be used as a sub rate</td>
</tr>
<tr>
<td></td>
<td>clock.</td>
</tr>
<tr>
<td>Clk Mod In</td>
<td>Input for delay modulation of the Trig Out and Clk Out channel. Both outputs</td>
</tr>
<tr>
<td></td>
<td>are always affected (SMA, female).</td>
</tr>
</tbody>
</table>
### Table 11  Sync In/Sync Out

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sync In</td>
<td>This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module.</td>
</tr>
<tr>
<td>Sync Out</td>
<td>This output is used to synchronize two or more modules to a common system clock. It is connected to the Sync In of the other module.</td>
</tr>
</tbody>
</table>

### Table 12  System Inputs/Outputs

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sys Out A/Sys Out B</td>
<td>System level control outputs used to signal events to the DUT or external instruments (SMA, female).</td>
</tr>
<tr>
<td>Sys In A/Sys In B</td>
<td>System level control inputs used to generate sequencer events (SMA, female).</td>
</tr>
</tbody>
</table>

### Table 13  Control Inputs/Output

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
</table>
| Ctrl In A/Ctrl In B| The module has two control inputs at the font panel each with the following selectable functionality (SMA, female):  
  **Error Add Input**  
  Every rising edge at the input generates a single error in the output data stream by flipping a single bit. The maximum repetition rate is data rate divided by 4 times the vector size.  
  **Output Blanking**  
  If the input level is above the threshold level the pattern generator stops and only O's are sent on data output. Normal operation resumes when the input level is below the threshold.  
  **Electrical Idle**  
  If the input level is above the threshold level the output amplifier enters electrical idle. Normal operation resumes when the input level is below the threshold.  
  **Gating Input**  
  If a logical high is applied to the gating input the error detector will ignore the incoming bits during a BER measurement. The ignored bit sequence is always a multiple of the vector size. For measuring data in bursts of bits, rather than a continuous stream of bits, a special operating mode is used. This mode is the burst sync mode. In this case, the signal at the gating input controls the synchronization and the error counting for each burst. |
| Ctrl Out A         | The module has one control output at the front panel with the following functionality (SMA, female):  
  **Error Output**  
  This signal can be used to trigger an external instrument to help in error analysis. If an error occurs, a single RZ pulse is generated. Continuous errors will result in a clock signal. |
J-BERT M8051A Generator-Analyzer

The J-BERT M8051A is an instrument module that can be installed into the M9505A 5-slot AXIe Chassis. This module occupies two slots and requires the M8041A module for proper operation.

The M8051A is a two channel Generator and two channel Analyzer for performing compliance and characterization measurements.

M8051A Features

The main M8051A features are the same as the M8041A features. For details, refer to J-BERT M8041A Generator-Analyzer-Clock Module on page 38.

M8051A Module Components

The following figure displays the front panel of the M8051A module with its various components labeled.
The M8051A module has the following components.

### Table 14  Insertion/Extraction and Retaining

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Retaining screws</td>
<td>The screws on both ends of the module are used to retain the module tightly inside the M9505A AXiE Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.</td>
</tr>
<tr>
<td>Module Insertion/Extraction Handles</td>
<td>The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXiE Chassis.</td>
</tr>
</tbody>
</table>

### Table 15  Front Panel LEDs

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Active when...</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fail</td>
<td>power-up fault condition</td>
<td>red</td>
</tr>
<tr>
<td>Access</td>
<td>power-up ready state</td>
<td>green</td>
</tr>
<tr>
<td>Data In x</td>
<td>input is overloaded</td>
<td>red</td>
</tr>
<tr>
<td>Data Out x</td>
<td>output is overloaded</td>
<td>red</td>
</tr>
<tr>
<td>Data Mod In x</td>
<td>input is active</td>
<td>green</td>
</tr>
<tr>
<td>Ctrl In A/Ctrl In B</td>
<td>logic level is detected</td>
<td>green</td>
</tr>
</tbody>
</table>

**M8051A Front Panel Connector Inputs/Outputs**

**CAUTION** The inputs of the M8051A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.
Table 16  Channel x Data Inputs/Outputs

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Out and /Data Out</td>
<td>Differential data outputs (3.5 mm, female).</td>
</tr>
<tr>
<td>Data In and /Data In</td>
<td>Differential data inputs (3.5 mm, female).</td>
</tr>
<tr>
<td>Data Mod In</td>
<td>Accepts an external source for data out delay modulation (SMA, female).</td>
</tr>
</tbody>
</table>

Table 17  Sync In

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sync In</td>
<td>This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module or to the clock distribution module if more than two modules are installed. The sync cable is required if M8051A is connected with M8041A module.</td>
</tr>
</tbody>
</table>

Table 18  Control Inputs/Output

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
</table>
| Ctrl In A/Ctrl In B| The module has two control inputs at the front panel each with the following selectable functionality (SMA, female):  
|                   | Error Add Input  
|                   | Every rising edge at the input generates a single error in the output data stream by flipping a single bit. The maximum repetition rate is data rate divided by 4 times the vector size.  
|                   | Output Blanking  
|                   | If the input level is above the threshold level the pattern generator stops and only 0's are sent on data output. Normal operation resumes when the input level is below the threshold.  
|                   | Electrical Idle  
|                   | If the input level is above the threshold level the output amplifier enters electrical idle. Normal operation resumes when the input level is below the threshold.  
|                   | Gating Input  
|                   | If a logical high is applied to the gating input the error detector will ignore the incoming bits during a BER measurement. The ignored bit sequence is always a multiple of the vector size. For measuring data in bursts of bits, rather than a continuous stream of bits, a special operating mode is used. This mode is the burst sync mode. In this case, the signal at the gating input controls the synchronization and the error counting for each burst.  

| Ctrl Out A         | The module has one control output at the front panel with the following functionality (SMA, female):  
|                   | Error Output  
|                   | This signal can be used to trigger an external instrument to help in error analysis. If an error occurs, a single RZ pulse is generated with the width of half a vector length. Continuous errors will result in a clock signal. |
M8061A 32 Gb/s Multiplexer with De-emphasis Module

The M8061A is an instrument module that can be installed into the M9502A 2-slot or M9505A 5-slot AXiLe Chassis. This module occupies two slots.

The M8061A is used to characterize serial interfaces of up to 32 Gb/s. The M8061A provides four calibrated de-emphasis taps, which can be extended to eight taps, built-in superposition of level interference, and Clock/2 jitter injection.

M8061A Features

- Expands data rate of M8041A and M8051A generators up to 32 Gb/s enabling accurate and complete receiver stress testing
- Integrated and calibrated 4-tap de-emphasis, expandable to 8 taps
- Internal superposition of interference for common mode and differential mode
- Transparent to jitter generated by the J-BERT M8020A, Clock/2 jitter can be added
- Supports electrical idle
- Control from J-BERT M8020A user interface via USB.

M8061A Module Components

The following figure displays the front panel of the M8061A module with its various components labeled.
The M8061A module has the following components.

### Table 19  Insertion/Extraction and Retaining

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Retaining screws</td>
<td>The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.</td>
</tr>
<tr>
<td>Module Insertion/Extraction Handles</td>
<td>The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.</td>
</tr>
</tbody>
</table>

### Table 20  Front Panel LEDs

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Active when...</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fail</td>
<td>power-up fault condition</td>
<td>red</td>
</tr>
<tr>
<td>Access</td>
<td>power-up ready state</td>
<td>green</td>
</tr>
</tbody>
</table>
M8061A Front Panel Connector Inputs/Outputs

**CAUTION**  
The inputs of the M8061A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

<table>
<thead>
<tr>
<th>Table 21</th>
<th>Electrical Idle Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
<td>Description</td>
</tr>
<tr>
<td>Electrical Idle In</td>
<td>This input is used to enable/disable the output signal by an external control signal. If the input level is above the threshold level the module enters electrical idle. Normal operation resumes when the input level is below the threshold (SMA, female).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 22</th>
<th>Clock Inputs/Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
<td>Description</td>
</tr>
<tr>
<td>Clk Out</td>
<td>Reference clock output used in clean clock mode to provide the synthesizer signal to the J-BERT without external splitter (3.5 mm, female).</td>
</tr>
<tr>
<td>Clk In</td>
<td>Reference clock input used in clean clock mode, the synthesizer should be connected to this port (3.5 mm, female).</td>
</tr>
<tr>
<td>Aux Clk In</td>
<td>External clock input in the range of 150 MHz to 14.2 GHz. This input is used with the J-BERT's internal clock. In presence of jitter, this provides the same jitter as the data outputs (3.5 mm, female).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 23</th>
<th>DMI/CMI Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
<td>Description</td>
</tr>
<tr>
<td>DMI In</td>
<td>Differential mode interference input independent of ground (SMA, female).</td>
</tr>
<tr>
<td>CMI In</td>
<td>Common mode interference input relative to ground (SMA, female).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 24</th>
<th>Data Inputs/Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
<td>Description</td>
</tr>
<tr>
<td>Data Out and /Data Out</td>
<td>Differential or single-ended data output (2.4 mm, female).</td>
</tr>
<tr>
<td>Data In x</td>
<td>Single-ended data input (3.5 mm, female).</td>
</tr>
</tbody>
</table>
M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

The M8062A extends the data rate of the J-BERT M8020A Bit Error Ratio Tester to the speeds required for testing devices with lane rates in the 25-28 Gb/s range. When combined with a two channel M8041A, the system provides data pattern generation and full-rate error analysis for users and systems with lane rates up to 32.4 Gb/s.

M8062A Features

- Extends maximum data rate of J-BERT M8020A up to 32.4 Gb/s
- Seamless control of pattern generator and error analyzer
- Integrated 8-tap de-emphasis
- Built in ISI generator for channel emulation
- Analyzer equalization eliminates errors resulting from closed eyes in loop back path
- Built in CDR for data rates up to 32 Gb/s

**NOTE**

The CDR license (M8062A-0A4) is required to enable the CDR feature. M8062A modules with serial numbers < MY55400300 may also require a hardware upgrade in order to enable this feature.

Refer to the Online Help installed and integrated into the M8070B software to learn about how to use this module.

**NOTE**

Phase-matched cables must be used when connecting the M8041A data and clock outputs to the M8062A data and clock inputs. The provided cable set, Keysight M8062-61643, meets this requirement.
M8062A Module Components

The following figure displays the front panel of the M8062A module with its various components labeled.

The M8062A module has the following components.

Table 25  Insertion/Extraction and Retaining

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Retaining screws</td>
<td>The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.</td>
</tr>
<tr>
<td>Module Insertion/Extraction Handles</td>
<td>The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.</td>
</tr>
</tbody>
</table>

Table 26  Front Panel LEDs

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Active when...</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fail</td>
<td>power-up fault condition</td>
<td>red</td>
</tr>
<tr>
<td>Access</td>
<td>power-up ready state</td>
<td>green</td>
</tr>
</tbody>
</table>

CAUTION  The inputs and outputs of the M8062A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.
Table 27  Sync In/Clean Clk Out

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sync In</td>
<td>This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module. The sync cable is required if M8062A is connected with M8041A module.</td>
</tr>
<tr>
<td>Clean Clk Out</td>
<td>Half-rate, or divided, clock output with no applied jitter.</td>
</tr>
</tbody>
</table>

M8062A Front Panel Pattern Generator Connectors

Table 28  Electrical Idle Input

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Idle In</td>
<td>This input is used to enable/disable the output signal by an external control signal. If the input level is above the threshold level the module enters electrical idle. Normal operation resumes when the input level is below the threshold (SMA, female).</td>
</tr>
</tbody>
</table>

Table 29  Pattern Generator Clock Inputs/Output

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clk Out</td>
<td>Half-rate Pattern Generator clock output. Carries the same jitter as the full-rate data output.</td>
</tr>
<tr>
<td>Clk In</td>
<td>Pattern Generator clock input (half-rate). Connect to clock output of M8041A.</td>
</tr>
<tr>
<td>Aux Clk In</td>
<td>Alternate Pattern Generator clock input (half-rate). Typically unused.</td>
</tr>
</tbody>
</table>

Table 30  DMI/CMI Inputs

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMI In</td>
<td>Differential Mode Interference input. Applies a single-ended, external interference source differentially to the data output (SMA, female).</td>
</tr>
<tr>
<td>CMI In</td>
<td>Common Mode Interference input. Applies a single-ended, external interference source to both the normal and complement data output signals (SMA, female).</td>
</tr>
</tbody>
</table>
## M8062A Front Panel Analyzer Connectors

### Table 31  Pattern Generator Data Inputs/Outputs

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Out and /Data Out</td>
<td>Differential or single-ended, full-rate data output to the device under test. Unused outputs must be terminated into 50 Ω (2.4 mm, female).</td>
</tr>
<tr>
<td>Data In 1 and Data In 2</td>
<td>Single-ended, half-rate data inputs from the M8041A module (3.5 mm, female).</td>
</tr>
</tbody>
</table>

### Table 32  Error Analyzer Data Inputs/Outputs

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data In and /Data In</td>
<td>Differential or single-ended, full-rate data input from the device under test. Unused input should be terminated into 50 Ω (2.4 mm, female). These ports are AC coupled.</td>
</tr>
<tr>
<td>Data Out 1 and Data Out 2</td>
<td>Single-ended, half-rate data outputs to the M8041A module (3.5 mm, female).</td>
</tr>
</tbody>
</table>

### Table 33  Error Analyzer Clock Inputs/Output

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clk Out</td>
<td>Half-rate Error Analyzer clock output, synchronous with analyzer sampling.</td>
</tr>
<tr>
<td>Clk In</td>
<td>Half-rate, Error Analyzer clock input. Allows external clocking of the Error Analyzer.</td>
</tr>
</tbody>
</table>
M8020A Module Setup

M8020A being a modular product includes different sets of modules which are hosted in an AXI chassis. It comprises of exactly one M8041A generator-analyzer-clock module and optionally one additional M8051A generator-analyzer module. The M8041A generator-analyzer-clock module is a true superset of the M8051A generator-analyzer module.

Setting up a Single Channel System

The single channel system is the smallest configuration consisting of one M8041A generator-analyzer-clock module within a 5-slot frame. You can upgrade it to a 2 channel system by adding the two channel options (second channel generator and second channel analyzer).

Setting up a Multi-Channel System

The multi-channel system is comprised of exactly one clock/data module and one or more data channels mounted in an AXIe frame.

The multi-channel system can be:

2-Channel System

A two-channel system consists of one clock/data module.

The following figure illustrates a two-channel system.
4-Channel System

A four-channel system consists of one clock module and one data modules.

The following figure illustrates a four-channel system.

For more details on how to establish connections between the M8020A modules, refer to the M8020A/M8030A Installation Guide.
M8030A Module Setup

The M8030A is a modular test solution which can be tailored to your specific needs from two channels with one M8041A to up to 10 channels. The modules must be installed in the M9514A AXIe 14-slot chassis as described in Table 34 on page -55:

<table>
<thead>
<tr>
<th>Slot Number</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td># 1</td>
<td>M8030A-BU1 AXIe embedded controller.</td>
</tr>
<tr>
<td># 2, 3 &amp; 4</td>
<td>M8041A module</td>
</tr>
<tr>
<td># 5 &amp; 6</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 7</td>
<td>M9521A AXIe system module</td>
</tr>
<tr>
<td># 8 &amp; 9</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 10 &amp; 11</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 12 &amp; 13</td>
<td>M8051A module</td>
</tr>
<tr>
<td># 14</td>
<td>M8192A multi-channel synchronization module</td>
</tr>
</tbody>
</table>
M8030A Modules Arrangement Example

The following figure shows the M8030A modules arrangement in the M9514A AXiE 14-slot chassis:
M8040A Overview

The M8040A is a modular instrument which supports the following modules:

- M8045A High-Performance BERT Pattern Generator-Clock
- M8046A High-Performance BERT Analyzer
- M8057A/B Pattern Generator Remote Head

M8040A being a modular product includes different sets of modules which are hosted in an AXI chassis. Each module and its features have their own license. You need to install these options in your instrument in order to use the modules or features. For details, refer to the chapter Licenses on page 547. However, if you have ordered M8040A-BU1, no license is required.

For details on the features and hardware components of each of the above mentioned modules, refer to M8040A Getting Started Guide.

**NOTE**

In case an AWG module (M8195A/M8196A) is used in a combined system with M8040A modules, ensure that the AWG modules should be always be mounted in a slot number higher that M8040A modules in the AXIe chassis. In other words, an AWG module always has to mounted last in the chassis.
M8040A Modules

M8045A High-Performance BERT Pattern Generator-Clock Module

The M8045A module can be a one or two data channel system (a second channel can be added with license). A one channel instrument has to be returned to the factory for installing the second channel (hardware) and license. It occupies three slots of the 5-slot M9505A AXIe chassis.

M8045A Features

- Up to two Pattern Generator channels per 3-slot-module
- Symbol rate 2 to 64 Gbaud
- NRZ and PAM4 format is software-selectable
- PAM4 up to 64 Gbaud
- Built in de-emphasis
- Built in and calibrated jitter generation
- External jitter modulation per channel
- Remote head to get close to the DUT
- Pattern memory, PRBS, pattern sequencing
- Sequencing control by external control signals

Refer to the Online Help installed and integrated into the M8070B software to learn about how to use this module.

M8045A Module Components

The following figure displays the front panel of the M8045A module (2 data channel system):
The M8045A module has the following components.

Table 35  Insertion/Extraction and Retaining

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Retaining screws</td>
<td>The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.</td>
</tr>
<tr>
<td>Module Insertion/Extraction Handles</td>
<td>The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.</td>
</tr>
</tbody>
</table>

Table 36  Front Panel LEDs

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Active when...</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fail</td>
<td>power-up fault condition</td>
<td>red</td>
</tr>
<tr>
<td>Access</td>
<td>power-up ready state</td>
<td>green</td>
</tr>
<tr>
<td>Data Mod In 1/2</td>
<td>signal is detected</td>
<td>green</td>
</tr>
<tr>
<td>Clk Out 1/2</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Ctrl Out 1/2</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Ctrl In 1/2</td>
<td>logic level is detected</td>
<td>green</td>
</tr>
<tr>
<td>P &amp; N 1/2</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Clk In</td>
<td>signal is detected</td>
<td>green</td>
</tr>
<tr>
<td>Ref Clk In</td>
<td>signal is detected</td>
<td>green</td>
</tr>
<tr>
<td>Ref Clk Out</td>
<td>Outputs a 10 and 100 MHz clock, 1 Vpp single ended into 50 Ohm</td>
<td>green</td>
</tr>
<tr>
<td>Aux In</td>
<td>not used</td>
<td>n/a</td>
</tr>
<tr>
<td>Clk Out</td>
<td>output is active</td>
<td>green</td>
</tr>
<tr>
<td>Trig Out</td>
<td>output is active</td>
<td>green</td>
</tr>
</tbody>
</table>
CAUTION

The inputs/outputs of the M8045A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Table 37  M8045A Front Panel Input/Output Ports

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| Clk Out 1, 2   | • Low Jitter (~150fs) Clk out. Baud-rate / 1,2,4,8,16  
                 • Same Jitter as Data out or clean clk  
                 • Typ 1.5 V pp  
                 • Used for Analyzer as external clock |
| P and N        | P and N must be connected to M8057A/B remote head. |
| Remote Head 1, 2 | Remote Head Control. This output provides power and control signals for the remote head amplifier |
| Data Mod In 1, 2 | This input is used for data out delay modulation by an external source. |
## Ctrl In A, B
The data module has 2 control inputs at the front panel. The functionality of each individual input can be selected.
- **Error Add Input**
  Every rising edge at the input generates a single error in the output stream by flipping a single bit. The maximum repetition rate is data rate divided by 4 times the vector size.
- **Output Blanking**
  If the input level is above the threshold level pattern generation stops and only 0’s are sent on data out. Normal operation resumes when the input level is below the threshold.
- **Electrical Idle**
  If the input level is above the threshold level the output amplifier enters electrical idle. Normal operation resumes when the input level is below the threshold.

## Ctrl Out A, B
The data module has 2 control output at the front panel.
- **Ctrl Out A** is the control output of channel 1.
- **Ctrl Out B** is the control output of channel 2.
- A pattern sequence that is using CTRL OUT A or CTRL OUT B will always drive all the control outputs of the channels that execute the pattern sequence. For independent control of Ctrl Out A and B, use independent sequences for channel 1 and 2.

## Sync Out A, B
This output is used to synchronize two or more modules to a common system clock. It is connected to the SYNC IN of the other module or to the M8192A if more than two modules are used.

## Clk In
Clock not used for M8045A.

## Ref Clk In
Reference clock input for applications that provide a host reference clock in the range of 10 MHz ... 16 GHz. It may be SSC modulated and is used as the reference for the system clock of all TX and RX channels. A SSC tolerant PLL is used to multiply the reference clock to the system clock.

## Ref Clk Out
The reference clock output is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment.

## Aux In
Port not in use.

## Clk Out
Differential clock output.

## Trig Out
This output is used to send a trigger signal to another connected device, such as an oscilloscope.

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| Ctrl In A, B   | The data module has 2 control inputs at the front panel. The functionality of each individual input can be selected.  
- Error Add Input  
  Every rising edge at the input generates a single error in the output stream by flipping a single bit. The maximum repetition rate is data rate divided by 4 times the vector size.  
- Output Blanking  
  If the input level is above the threshold level pattern generation stops and only 0’s are sent on data out. Normal operation resumes when the input level is below the threshold.  
- Electrical Idle  
  If the input level is above the threshold level the output amplifier enters electrical idle. Normal operation resumes when the input level is below the threshold. |
| Ctrl Out A, B  | The data module has 2 control output at the front panel.  
- Ctrl Out A is the control output of channel 1.  
- Ctrl Out B is the control output of channel 2.  
- A pattern sequence that is using CTRL OUT A or CTRL OUT B will always drive all the control outputs of the channels that execute the pattern sequence. For independent control of Ctrl Out A and B, use independent sequences for channel 1 and 2. |
| Sync Out A, B  | This output is used to synchronize two or more modules to a common system clock. It is connected to the SYNC IN of the other module or to the M8192A if more than two modules are used. |
| Clk In         | Clock not used for M8045A. |
| Ref Clk In     | Reference clock input for applications that provide a host reference clock in the range of 10 MHz ... 16 GHz. It may be SSC modulated and is used as the reference for the system clock of all TX and RX channels. A SSC tolerant PLL is used to multiply the reference clock to the system clock. |
| Ref Clk Out    | The reference clock output is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment. |
| Aux In         | Port not in use. |
| Clk Out        | Differential clock output. |
| Trig Out       | This output is used to send a trigger signal to another connected device, such as an oscilloscope. |
The M8046A is an instrument module that can be installed into the M9505A 5-slot AXIe chassis. This module occupies one slot.

The M8046A supports symbol rates up to 32.4 Gbaud, the default is NRZ format.

The analyzer module can be used for error analysis in conjunction with the M8045A pattern generator, the M8195A/M8196A Arbitrary Waveform generators or as stand-alone.

With M8070B, the M8046A can also be used in conjunction with M8041A + M8062A.

The three or four channel configuration requires a cable (provided with the M8046A) that connects the M8045A Sync Out to the M8046A Sync In to synchronize the two modules to a common system clock. The M8046A Analyzer module can also be used with an external clock coming from CR (e.g. N1076A) or Generator output (M8045A channel 1/2 Clock Output or M8195A/M8196A Data Output).

### M8046A Features

- Symbol rates 2 to 32.4 Gbaud
- One channel per 1-slot module
- 70 mV input sensitivity
- Supports NRZ and PAM4
- Built-in equalization
- Real-time bit error and symbol error analysis
M8046A Module Components

The following figure displays the front panel of the M8046A module with its various components:

The M8046A module has the following components.

Table 38  Insertion/Extraction and Retaining

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Retaining screws</td>
<td>The screws on both ends of the module are used to retain the module tightly</td>
</tr>
<tr>
<td></td>
<td>inside the M9505A AXIe Chassis slot once you have fully placed it inside the</td>
</tr>
<tr>
<td></td>
<td>chassis. To remove the module, you first need to loosen these screws ensuring</td>
</tr>
<tr>
<td></td>
<td>that these screws disengage completely.</td>
</tr>
<tr>
<td>Module Insertion/Extraction Handles</td>
<td>The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.</td>
</tr>
</tbody>
</table>

Table 39  Front Panel LEDs

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Active when...</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fail</td>
<td>power-up fault condition</td>
<td>red</td>
</tr>
<tr>
<td>Access</td>
<td>power-up ready state</td>
<td>green</td>
</tr>
<tr>
<td>Clk In</td>
<td>on when output active and CLK detected</td>
<td>green</td>
</tr>
<tr>
<td>Ctrl Out</td>
<td>on when output active</td>
<td>green</td>
</tr>
<tr>
<td>Ctrl In</td>
<td>logic state is detected</td>
<td>green</td>
</tr>
<tr>
<td>Data In</td>
<td>data received</td>
<td>green</td>
</tr>
</tbody>
</table>
M8046A Front Panel Inputs/Outputs Ports

**CAUTION**
The inputs of the M8046A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data In and /Data In</td>
<td>Differential data inputs (3.5 mm, female)</td>
</tr>
<tr>
<td>Clk In</td>
<td>Clock input to sample the incoming data. Full/half and quarter-rate clock. Single ended.</td>
</tr>
<tr>
<td>Sync In</td>
<td>This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module or to the clock distribution module if more than two modules are installed. The sync cable is required if M8046A is connected with M8045A Pattern Generator module. Not needed if external clock is used.</td>
</tr>
<tr>
<td>Ctrl Out A</td>
<td>Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.</td>
</tr>
<tr>
<td>Ctrl In A</td>
<td>This input can be used as sequence trigger or pattern capture event.</td>
</tr>
</tbody>
</table>

**M8057A/B Pattern Generator Remote Head**
The M8057A/B remote head is an external box which must be connected to each channel of M8045A module. The three cables are fixed on the back side of M8057A/B which need to be connected to M8045A remote head, P and N connectors. It helps in minimizing signal degradations caused by lossy channels.

**NOTE**
Please note that it is mandatory to connect M8057A/B remote head with each channel of M8045A module. Operation without M8057A/B remote head will not allow you to receive data.
M8057A/B Remote Head Components

The following figure displays the front panel of the M8057A remote head with its various components. The similar front panel components are also available on the M8057B remote head.

The M8057A/B remote head has the following components.

Table 41 Front Panel LEDs

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Active when...</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ready</td>
<td>remote head is operation</td>
<td>green</td>
</tr>
</tbody>
</table>

Table 42 M8057A/B Front Panel Inputs/Outputs Ports

<table>
<thead>
<tr>
<th>Connector Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Out and /Data Out</td>
<td>Connected to DUT</td>
</tr>
</tbody>
</table>
The following figure displays the back panel of the M8057A/B remote head with its various components:

The back panel of M8057A/B remote head has cables which connects with each channel of M8045A remote head controls (P and N). The length of these cables are 85 cm.

Ensure that the chassis is NOT powered up or connected to a power source while making connections to M8057A/B.

Also, make sure NOT to remove the M8057A/B connections when it is powered on. However, if you wish to remove the M8057A/B connections, ensure that the instrument is powered off.
M8040A Module Setup

The M8040A 64Gbaud BERT is based on individual modules that are controlled by the M8070B software. The modules must be hosted in the 5-slot AXI chassis as described below:

- The M8045A module occupies three slots of the 5-slot M9505A AXIe chassis. It must be installed in slots 1 through 3 in the AXIe chassis unless the M9537A AXIe Embedded Controller is installed. The M9537A AXIe Embedded Controller must be installed in slot 1.
- The M8046A module occupies a single slot of the 5-slot M9505A AXIe chassis.
- The M8057A/B remote head is an external box which must be connected to each channel of M8045A module. Three cables are fixed on the back side of M8057A/B which need to be connected to M8045A remote head, P and N connectors.

The following figure shows a typical setup of M8045A, M8046A and M8057A/B.
M8070B Supported Plugins

The M8070B system software supports the following plugins:

- **Advanced Measurement Package** - The Advanced Measurement Package provides the following measurements:
  - Output Timing
  - Output Level
  - Jitter Tolerance
  - Eye Diagram
  - Parameter Sweep

  For details on the measurements provided by **Advanced Measurement Package**, please refer to **M8000 Series Advanced Measurement Package User Guide**.

- **Error Distribution Analysis Package** - The Error Distribution Analysis Package provides the following measurement:
  - Error Distribution Analysis

  For details on the measurement provided by **Error Distribution Analysis Package**, please refer to **M8000 Series Error Distribution Analysis Package User Guide**.

These plugin files (*.M8KP) which can be downloaded from Keysight web page.

### NOTE

The Advanced Measurement Package and Error Distribution Analysis Package requires a valid license for activation. For details on license, refer to **Licenses** on page 547.

The M8070B software comes with a Plugin Manager to simplify all the tasks related to plugin management. The Plugin Manager can help you to install the plugins. For further details on how to install, update or uninstall plugins, please refer to the **Plug-in Manager** on page 540. Additionally, you can also refer to the **M8000 Series Plugins Getting Started Guide**.
AWG Modules Supported by M8070B System Software

In addition to the BERT modules, the M8070B system software also supports the following AWG modules:

- M8195A 65 GSa/s Arbitrary Waveform Generator
- M8196A 92 GSa/s Arbitrary Waveform Generator

**NOTE**

In case an AWG module (M8195A/M8196A) is used in a combined system with either M8020A or M8040A modules, ensure that the AWG modules are always mounted in a slot number, higher that M8020A or M8040A modules in the AXIe chassis. In other words, an AWG module always has to be mounted, last in the chassis.

M8195A 65 GSa/s Arbitrary Waveform Generator

The Keysight M8195A is a 65 GSa/s Arbitrary Waveform Generator with highest bandwidth and channel density. Flexible signal generation at up to 32 Gbaud. Clean and distorted signal to stress the device to the limits. High speed AWG with up to 65 GSa/s sample rate and 20 GHz bandwidth on up to 4 channels per module. The M8195A arbitrary waveform generator offers an output amplitude of up to 2 Vpp (diff.) and adjustable DC offset.

The M8195A module has 4 channels and up to 5 modules can be inserted in a 5 slot AXI chassis to provide the maximum of 20 channels. This is valid for channels which are not synchronized across module boundaries. To synchronize these modules, a sync module is added in the frame. Since the sync module occupies a single slot, only 4 AWG modules can now be added thereby providing a maximum of 16 channels in a frame.

The M8195A AWG gives you the versatility to create the signals you need for digital applications, optical and electrical communication and advanced research.

The basic functionality of the M8195A is controlled from a soft front panel application running on the AXIe embedded controller or external PC or laptop. However, the M8195A can also be integrated into the M8070B system software for M8000 Series of BER test solutions.

Details of M8195A module can be found at www.keysight.com/find/M8195A.
M8196A 92 GSa/s Arbitrary Waveform Generator

The Keysight M8196A is a 92 GSa/s Arbitrary Waveform Generator with highest bandwidth and channel density. It offers up to 4 x 512 kSa waveform memory. It is a high speed AWG with up to 96 GSa/s sample rate and 32 GHz bandwidth on up to 4 channels per module. The M8196A arbitrary waveform generator offers an output amplitude of up to 2 Vpp (diff.) and adjustable DC offset.

The M8196A provides high speed, precision, and flexibility which is ideally suited for digital applications, optical, aerospace/defense, and electrical communication.

The basic functionality of the M8196A is controlled from a soft front panel application running on the AXIe embedded controller or external PC or laptop. However, the M8196A can also be integrated into the M8070B system software for M8000 Series of BER test solutions.

Details of M8196A module can be found at www.keysight.com/find/M8196A.
M8054A Interference Source Module

The Keysight M8054A interference source module allows you to generate repeatable and accurate level impairments for testing of high-speed digital receivers that support symbol rates up to 64 Gbaud. The M8054A interference source module is controlled through the M8070B system software.

Key Features & Specifications

- Random level interference with crest factor > 4
- Sinusoidal level interference
- Common mode and differential mode
- Bandwidth adjustable up to 32 GHz
- 4 differential output channels to avoid baluns
- Adjustable amplitude up to 1 Vpp (se), 2 Vpp (diff.)
- 1-slot AXIe module for combined configurations with M8040A high-performance BERT
- Graphical user interface and remote control via M8070B system software for M8000 series of BER test solution

Details of M8054A module can be found at www.keysight.com/find/M8054A.
Other Supported Hardware(s)

Keysight N1076A/N1077A DCA-M Clock Recovery

The N1076A electrical clock recovery and N1077A electrical/optical clock recovery provide necessary clock signals to trigger an 86100D, N109x-series DCA-M oscilloscopes, or the error detector in a M8070B.

You can use an N1076/7A when:

- Access to appropriate clock signals from the Device Under Test (DUT) is not possible. The clock is recovered from the data stream.
- The existing clock has excessive intrinsic jitter that prevents accurate measurements. The N1076/7A can act as clean-up PLL for the clock.
- Input data is between 50 MBd and 16 Gbd (32 Gbd with option 232).

Detailed description of N1076A/N1077A can be found at:

www.keysight.com/find/N1076A
www.keysight.com/find/N1077A
The M8070B system software supports certain real-time oscilloscopes to measure BER of NRZ signals and BER as well as SER of PAM4 signals. The real-time oscilloscope is completely controlled from M8070B to capture a signal and convert into a pattern stream that is then uploaded into the M8070B for comparison with an expected pattern and provide BER/SER measurements.

Nevertheless, it is possible to stop measuring BER on the integrated oscilloscope and therefore allow interactive tweaking of oscilloscope settings before continuing the BER measurements.

Currently, the following oscilloscopes models are supported:

- DSOZ634A Infiniium Z-Series Digital Storage Oscilloscope 63GHz / 160Gsa/s
- DSAZ634A Infiniium Z-Series Digital Signal Analyzer 63GHz / 160Gsa/s
- DSOZ594A Infiniium Z-Series Digital Storage Oscilloscope 59GHz / 160Gsa/s
- DSAZ594A Infiniium Z-Series Digital Signal Analyzer 59GHz / 160Gsa/s
- DSOZ504A Infiniium Z-Series Digital Storage Oscilloscope 50GHz / 160Gsa/s
- DSAZ504A Infiniium Z-Series Digital Signal Analyzer 50GHz / 160Gsa/s
- DSOX96204Q Infiniium Q-Series Digital Storage Oscilloscope 63GHz / 160Gsa/s
- DSAX96204Q Infiniium Q-Series Digital Signal Analyzer 63GHz / 160Gsa/s
- UXR0334A 33GHz / 128GSa/s
- URX0402A 40GHz / 256GSa/s
- UXR0404A 40GHz / 256GSa/s
- UXR0502A 50GHz / 256GSa/s
- UXR0504A 50GHz / 256GSa/s
- UXR0592A 59GHz / 256GSa/s
- UXR0594A 59GHz / 256GSa/s
- UXR0592AP 59GHz / 256GSa/s
- UXR0594AP 59GHz / 256GSa/s
- UXR0702A 70GHz / 256GSa/s
- UXR0704A 70GHz / 256GSa/s
- UXR0702AP 70GHz / 256GSa/s
- UXR0704AP 70GHz / 256GSa/s
Know Your Hardware

- UXR0802A 80GHz / 256GSa/s
- UXR0804A 80GHz / 256GSa/s
- UXR1002A 100GHz / 256GSa/s
- UXR1004A 100GHz / 256GSa/s
- UXR1102A 110GHz / 256GSa/s
- UXR1104A 110GHz / 256GSa/s

Detailed description of the above oscilloscopes can be found at:
http://www.keysight.com/find/oscilloscopes

The following licenses are required on the oscilloscope:
- N5384A Serial Data Analysis (SDA)
- N8827A PAM4 Measurement (PM4)
- N5461A Equalization (DEQ)

NOTE

The minimum supported Infiniium version is 06.10.00616.
The minimum supported Infiniium UXR-Series version is 10.10.

For details on how to control a real-time scope from M8070B, refer to the
Hardware Setup for M8046A and M8062A Modules

The M8046A module and the M8062A module can be used in the same setup. The following are the supported configurations:

1. Two M9505A 5-slot AXIe chassis controlled via USB
   - **Chassis 1:**
     - Slot 1: M8041A
     - Slot 4: M8062A
   - **Chassis 2:**
     - Slot 1: M8046A
   USB control ports of both chassis connected to the controlling PC

2. Two M9505A 5-slot AXIe chassis using an embedded controller
   - **Chassis 1:**
     - Slot 1: M8041A
     - Slot 4: M8062A
   - **Chassis 2:**
     - Slot 1: Embedded Controller (M9536A or M9537A)
     - Slot 2: M8046A
   USB control port of chassis 1 is connected to a USB 2.0 port of the embedded controller

3. M9514A 14-slot chassis controlled from external computer
   - Slot 1: M8041A
   - Slot 4: M8062A
   - Slot 6: M8046A
   - Slot 7: M9521A AXIe System Module

4. M9514A 14-slot chassis controlled from embedded controller
   - Slot 1: Embedded Controller (M9536A or M9537A)
   - Slot 2: M8041A
   - Slot 5: M8062A
   - Slot 7: M9521A AXIe System Module
   Slot 8: M8046A
   The M8046A may be used with a N1076A external clock recovery.
Limitations

The following are the limitations while using the M8046A and M8062A modules in the same setup:

- The M8046A does not support all sequencer word width settings of a M8041A/M8062A combination.
- Even though M8041A/M8062A and M8046A support a common sequencer word width of 1, they internally work with a different granularity and therefore cannot be used in the same sequence. Instead individual sequences need to be defined for M8062A Data Out, Data In and M8046A.
- In order to run the M8062A Data Out and M8046A Data In at the same symbol rate, the CLK IN frequency of M8046A needs to be specified manually. To do this, disable ‘Follow SYS CLK’ under Clock and specify CLK IN frequency and multiplier as required for the setup.
ESD Protection

Electrostatic discharge (ESD) can damage the circuits of the components on M8020A/M8030A/M8040A modules (M8041A, M8051A, M8061A, M8062A, M8045A, M8046A and M8057A/B). Avoid applying static discharges to the front-panel connectors. Before connecting any coaxial cable to the connectors, momentarily short the center and outer conductors of the cable together. Avoid touching the front-panel connectors without first touching the frame of the instrument. Be sure the instrument and all connected devices (DUT, etc.) are properly earth-grounded (to a common ground) to prevent buildup of static charge and electrical over-stress. Take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Electrostatic discharge (ESD) can damage or destroy electronic components. All work on electronic assemblies should be performed at a static-safe work station. The following list and figure shows an example of a static-safe work station using two types of ESD protection. Purchase acceptable ESD accessories from your local supplier.

- Conductive table-mat and wrist-strap combination.
- Conductive floor-mat and heel-strap combination.
Both types, when used together, provide a significant level of ESD protection. Of the two, only the table-mat and wrist-strap combination provides adequate ESD protection when used alone. To ensure user safety, the static-safe accessories must provide at least 1 MW of isolation from ground.

**WARNING**

These techniques for a static-safe work station should not be used when working on circuitry with a voltage potential greater than 500 volts.
Discharging Cables

Loose cables are like a capacitor and can hold electrostatic charges. The free end of a cable touching surfaces that have voltage levels will cause product damage. Before connecting any cable to product connector, short the center and outer conductors of the cable together to ground momentarily.

You should use the cable discharger provided with the initial product shipment and shown in the following figures.
While discharging a cable, make sure to ground the box appropriately, via the “GND” connector of the box, to the ground connector of the AXIe chassis as shown in the figure.

That is either directly using the accessories provided with the discharger like the grounding cable, or via an ESD mat, which is connected to the ground connector of the AXIe chassis.

Discharge your cables using the matching connector e.g. 2.40 mm (also for 1.85 mm), 3.50 mm (also for 2.92 mm) and Mini-Coax. You may stick the cable discharger box to your instrument/AXIe chassis e.g. using the fastener tape provided.

Fixture made of plastic can store charges, and probing powered devices can subject inputs to damaging voltage and power levels. Poor AC power supply connected to product or DUT may create AC transients, insufficient grounding, floating neutral lines which cause damaging currents to flow into or out of the instrument.

For more information about electrostatic discharge, contact the Electrostatic Discharge Association www.esda.org.
Keysight M8000 Series of BER Test Solutions
User Guide

3 Quick Tour with M8070B User Interface

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Exploring M8070B User Interface  / 89
Other GUI Features  / 111
Recall/Save Instrument State  / 118
Overview

The M8070B system software for the M8000 Series of BER Test Solutions is required to control M8020A/M8030A/M8040A modules (M8041A, M8051A, M8061A, M8062A, M8045A, M8046A and M8057A/B) and other modules from M8000 family (M8190A, M8195A and M8196A). It provides a user-friendly experience that can be used with standard or touchscreen enabled computers. It is fully supported by the Microsoft Windows 7 (64 bit) SP1, Windows 8 (64 bit), Windows 8.1 (64 bit) and Windows 10 (Version 1607, Anniversary Update or newer) operating systems. The M8070B software also supports an off-line version, that does not require any license to operate.

The M8070B user interface provides an interactive graphical display in multiple windows containing controls, that enable you to perform the tasks. The GUI components include menus, tool bars, dialog boxes, toggle buttons, standard windows buttons, drop-down lists, sliders, and many more which are further discussed in this manual.

NOTE

Depending upon the M8020A/M8030A/M8040A bundle with of chassis/controller pre-installation, you may have to install the M8070B software. Refer to Installation Guide and follow the given instructions to install the M8070B software.
Launching M8070B User Interface

To launch the M8070B user interface, go to Start menu and then click All Programs > Keysight M8070B > Keysight M8070B.

The splash screen will be displayed as shown in the following figure:

![M8070B Splash Screen](image)

Messages while launching M8070B GUI

Whenever there is a change in the M8070B software version, the following message appears:
This message box prompts the user to update the workspace as there is an update in the software version.

- Clicking on “Yes” will update the workspace.
- Clicking on “No” will do nothing and you will have to manually update the workspace. For details on how to update the workspace, refer the “M8070B Release Notes”.

Whenever, an old workspace data (M8070A) is detected, the following message will appear:

- Clicking on “OK” will import the user settings, patterns and other resources of M8070A workspace to M8070B workspace.
Load Setting

Before the M8070B software is launched, a **Load Setting** dialog will appear which allows you to load settings.

The **Load Setting** dialog provides the following settings:

- **Last Used**: Launches the M8070B user interface with the last used settings.
- **Factory Preset**: Launches the M8070B user interface with factory default settings.
- **Select...**: Opens the **Recall Instrument State** dialog which allows you to load the M8070B user interface with the stored settings. For details, refer to **Recall Instrument State** on page 118.
- **Exit Application**: Terminates the M8070B application.

**NOTE**

The **Load Setting** dialog will appear each time the M8070B software is launched.

**NOTE**

A warning message will appear on the top of **Load Setting** dialog if the modules are offline. In this case, the results are simulated.
Once the settings are loaded, the M8070B software launches. The following figure shows the M8070B user interface when there is only one module connected to the M8020A/M8030A system.

![M8070B User Interface](image)

However, if there are two modules connected to the M8020A/M8030A system, the M8070B user interface will appear as shown in the following figure:
Get Module Information

You can get the module information that is connected to the M8020A/M8030A by clicking the icon present at the right side of each module. If properly connected, the module information will be shown as depicted in the following figure:
It provides the following information about the module:

- **Address** - Address of module, e.g. USB-PXI0::11::0::INSTR
- **Product Number** - Product no. of the module, e.g. M8041A
- **Serial Number** - Serial no. of the module, e.g. DE53C00061
- **Hardware Revision** - Hardware revision of module, e.g. 0

However, if you unable to get the module information, we suggest you to restart the M8070B software.

In the off-line mode, the icon will appear in the M8070B GUI.
Exploring M8070B User Interface

The M8070B user interface consists of the following GUI elements:

- Title Bar
- Menu Bar
- Main Window
- Status Bar

The detailed information on these GUI elements are described in the following sections.

Title Bar

The title bar contains an application icon, title, a context-sensitive help icon and standard buttons to minimize, maximize or to close the window.

The context-sensitive help icon provides information about the M8070B user interface relative to the task a user performs.

The title bar is shown in the following figure.

Menu Bar

The menu bar consists of various drop-down menus which provide access to different functions, and launch interactive GUI controls.

The menu bar includes the following drop-down menus:

- File
- Application
- System
- Clock
- Generator
- Analyzer
- Patterns
- Measurements
- Utilities
- Window
- Help
• Measurements
• Utilities
• Window
• Help
• Increase/Decrease Splitter Size

Each drop-down menu and their options are described in the following sections.

**File Menu**

The **File** menu provides the following selection:

- **Preset Instrument State...** - Opens the **Preset Instrument State** dialog.

This dialog allows you to:

- **Soft Preset** - For a **Soft Preset**, select the check box and then click **Preset** button. This option resets the instrument state to factory default settings. However, it retains current symbol width, opened windows and data stored in current setting such as patterns, templates and scripts.

- **Preset** - Resets the parameters to their default values. You can also perform a soft preset/preset to the instrument by sending *RST command in the SCPI panel. For details on *RST command, refer to **M8000 Series Programming Guide**.

- **Recall Instrument State...** - Opens the **Recall Instrument State** dialog which allows you to retrieve the user-defined settings or the factory settings.

For more details, refer to **Recall Instrument State** on page 118.
Quick Tour with M8070B User Interface

- **Save Instrument State**... - Opens the **Save Instrument State** dialog which allows you to save the current instrument state. For more details, refer to **Save Instrument State** on page 119.
- **Exit** - Closes the M8070B user interface.

**Application Menu**

The **Application** menu allows you to select application specific features for the following:

- PCI Express
- USB
- SATA
- MIPI C-PHY/D-PHY (Included in separately available MIPI plug-in)
- 10 GBASE KR Link Training (For details, refer to the **10 GBASE KR Link Training User Guide**)

On selecting any of these standards from the **Application** menu, a standard specific dialog or plug-in interface will appear.

**System Menu**

The **System** menu allows you to launch the various display views provided by M8020A/M8030A/M8040A. It provides the following selections:

- **Module View** - Opens the **Module View** user interface as shown in the following figure:
The **Module View** is a graphical representation of the input/output ports that are present on the front panel of the modules, connected to the M8020A/M8030A. You can use the Module View to configure the properties of a single port or a group (combination of multiple ports). For details, refer to Module View on page 123.

- **System View** - Opens the **System View** user interface as shown in the following figure:

![System View](image)

The **System View** displays the block representation of the currently selected channel of the M8020A/M8030A/M8040A. In addition, it also allows you to interactively modify the configuration settings for each channel. For details, refer to System View on page 153.
• **Groups View** - Opens the **Group View** user interface as shown in the following figure:

![Groups View](image)

The **Group View** allows you to create a group of ports and re-program their properties. For details, refer to **Group View** on page 182.

• **Ctrl In/ Ctrl Out** - Opens the **Module View** with the Ctrl In/Ctrl Out ports selected and the corresponding parameters are reflected in the Properties window.

• **Sys In/Out A/B** - Opens the **Module View** with the Sys In/Out ports selected and the corresponding parameters are reflected in the properties window.

**Clock Menu**

The **Clock** menu provides the following selections:

• **Clock Generator** - Allows you to configure **Clk Gen** port.

• **Clock Output** - Allows you to configure **Clk Out** port.

Once you make a selection, the **Module View** appears with the **Clk Gen/Clk Out** ports selected and the corresponding parameters are reflected in the Properties window.
The following figure shows the **Module View** with the **Clk Gen** port selected:

The generator's output ports are used to supply a clock signal and trigger for another device (for example, analyzer), and an arbitrary data signal for testing your device. For details, refer to **Setting up Generator** on page 235.

To change bit rate, go to the **Properties** window and then click on the **Synthesizer** function block.

**Generator Menu**

The **Generator** menu provides the following selections:

- **Data Output** - Allows you to configure **Data Out** port.
- **Trigger Out** - Allows you to configure **Trig Out** port.

Once you make a selection, the **Module View** shows the **Data Out/Trig Out** ports selected and the corresponding parameters are reflected in the **Properties** window.
The following figure shows the Module View with the Data Out port selected:

The generator's ports are used to set the clock frequency and the output signal with respect to jitter, error insertion and signal output. For details, refer to Setting up Generator on page 235.

To change amplitude/offset, go to Properties window and then click the Amplifier function block.

Analyzer Menu

The Analyzer menu provides the following selections:

- Data Input - Allows you to configure Data In port.

Once you make a selection, the Module View shows the Data In ports selected and the corresponding parameters are reflected in the Properties window.
The following figure shows the **Module View** with the **Data In** port selected:

The analyzer's ports are used for running tests and for connecting external equipment. For details, refer to **Setting up Analyzer** on page 329.

**Patterns Menu**

The **Patterns** menu provides the following selections:

- **Select Pattern...** - Opens the **Select Sequence Pattern** dialog. It allows you to override all sequences with a single block loop. For details refer to **Pattern Editor** on page 425.
- **Pattern Editor** - Opens the **Pattern Editor** user interface as shown in the following figure:
The pattern editor provides an interactive user-interface for creating, editing and importing patterns. For details, refer to Pattern Editor on page 425.

- **Sequence Editor** - Opens the Sequence Editor user interface as shown in the following figure:
The **Sequence Editor** allows you to create and maintain sequences. In addition to this, it also allows you to edit the memory patterns. For details, refer to **Sequence Editor** on page 389.

**Measurements Menu**

The **Measurements** menu provides the following selections:

- **Error Ratio** - Opens the **Error Ratio** measurement user interface as shown in the following figure:

The error ratio measurement allows you to collect measurement data over a specific period. This can be used to create test scenarios that are reproducible and comparable. Also, you can let tests run over long times and then evaluate the results afterwards. For details, refer to **Error Ratio Measurement** on page 515.

**Utilities Menu**

The **Utilities** menu provides the following selections:

- **Self Test** - Opens the **Self Test** utility user interface as shown in the following figure:
The **Self Test** utility checks the specific system information of the hardware components for basic functionality. On execution, the following results are displayed:

- System related information such as connected modules, serial no. and hardware revision.
- Module related information such as calibration, power supplies and memory controller.

For details, refer to **Self Test Utility** on page 529.

- **Licenses...** - Opens the **Licenses** window user interface as shown in the following figure:
The **Licenses** window displays the license information currently installed in the modules or host. For details, refer to Licenses Window on page 534.

- **Settings...** - Opens the Settings window which allows you to set the display and channel settings in the user interface. For details, refer to Settings Window on page 535.

- **Logger** - The Logger window displays errors, warnings and information messages along with their respective descriptions, applications from where they are generated and their time stamps. For details, refer to Logger Window on page 538.

- **Plug-in Manager** - The **Plug-in Manager** simplifies all the tasks related to plug-in management. It displays list of plug-ins that are installed in the software. In addition, the **Plug-in Manager** also allows you to install, uninstall and update the plug-ins. For details, refer to Plug-in Manager on page 540.
Window Menu

The **Window** menu allows you to change the layout/arrangement of various open windows. It includes the following selections:

- **Cascade** - Arranges the multiple opened windows in a docked view so that you can see all or part of each window; consisting of individual tabs for each window.

The following figure shows the docked/tabbed view of three different windows.

- **Tile Horizontally** - Aligns the multiple opened windows in a horizontal sequence. The following figure shows the horizontal sequence of three different windows.
- **Tile Vertically** – Aligns open windows in a vertical sequence. The following figure shows the vertical sequence of three different windows.
- **Focus Center Content** - Minimizes or hides additional dialog boxes or property sheets of the multiple open windows to focus on the center content.
- **Close All** - Closes all the open windows.
Help Menu

The Help menu includes the following selections:

- **Help Contents (F1)** - Opens the online help that provides the information about the Keysight M8070B.

- **License Manager** - Opens the Keysight License Manager window, which allows you to manage node-locked and transportable licenses for a variety of software products and instruments. For more information, refer to Keysight License Manager 5 on page 564.

- **License Manager 6** - Opens the Keysight License Manager 6 window, which allows you to manage floating and USB portable licenses for a variety of software products and instruments. For more information, refer to Keysight License Manager 6 on page 563.
• **About M8070B** - Shows the product information of M8070B including version number, build date, build info and web links for M8070B information and support.

![About Keysight M8070B](image)

**Increase/Decrease Splitter Size**

The **Splitter** option allows you to either increase or decrease the divided space between the windows forms used in the user interface. This icon is located on the right side of the menu bar. The splitter functionality provides an easy navigation to the users who are using a touchscreen interface.

**Main Window**

The main window refers to the middle area of the M8070B user interface that allows you to launch different display views (e.g. **Module View**, **Group View**, **System View**, etc.). You can use the menu bar to launch these views on the main window. Each view can be configured through the **Parameters** window. The detailed description of different views, their parameter settings, controls and dialogs are described in the subsequent sections in this manual.

When you launch the M8070B software, by default, it shows the **Module View** on the main window.
The following figure shows how the main window appears:

![Main Window Screenshot]

Status Bar

The status bar is located at the bottom of the M8070B user interface. The status bar is shown in the following figure:

![Status Bar Screenshot]

It provides the following functions:

- Button to show/hide the **Status Indicator** window. For details, refer to [Status Indicators Window](#) on page 107.
- Button to show/hide the **Logger** window that displays errors, warnings and information messages which are generated from the M8020A/M8030A/M8040A system. For details, refer to [Logger Window](#) on page 109.
- Button to show/hide the **Show Link Training Log** window. For details, refer to [Link Training Log Window](#) on page 110.
- Error indicator for the clock loss. When there is any clock loss, the respective indicator turns red.
• Toggle button to enable/disable the **Global Outputs** and check-boxes to enable/disable the **Impairments** and **SSC** state.

• **Progress Indicator** to visualize the progression of multiple GUI operations and/or background operations in a single bar. However, if the process takes too long to complete, you have an option to terminate that process by clicking on the **Abort** button which appears on the **Status Bar**.

**NOTE**

The behavior of progress indicator depends upon the number of process involved in any operation. It displays progress of each individual process in a single bar. Time for each operation may vary and sometimes may be very quick. Therefore, at some instance, it may display a progress to be complete (100%) and then suddenly switch to incomplete (50%).

**WARNING**

You will see a warning sign on the status bar if the “Global Output State” is off. In this case, all data outputs will be disabled until the “Global Output State” is turned on. Click the “Output” button present on the status bar to turn on the “Global Output State”.

**NOTE**

The behavior of progress indicator depends upon the number of process involved in any operation. It displays progress of each individual process in a single bar. Time for each operation may vary and sometimes may be very quick. Therefore, at some instance, it may display a progress to be complete (100%) and then suddenly switch to incomplete (50%).

• **Insert Error** button to insert a single bit error on each Data Out location of the connected modules.

• **Preset All** button opens the **Preset Instrument** dialog that allows to reset the instrument state to factory default settings.

**Status Indicators Window**

The **Status Indicators** window displays the status indicators for the generator and analyzer ports of each channel of the connected modules. This includes:

• Setup information such as **Bit Rate** for each channel of the connected module.

• Generator port information such as:
  - Data information that shows the name/type of the pattern downloaded to that data block and its indicator shows which data block is currently transmitting the sequence.
  - State information of generator such as **Output**, **Jitter** and **SSC** (indicated by green LED).
Error indicator for the current GUI state. When the current GUI is stopped, the respective indicator turns red.

Analyzer port information such as:
- Data information that shows the name/type of the pattern downloaded to that data block and its indicator shows which data block is currently transmitted the sequence.
- State information of analyzer such as BRM (indicated by green LED).
- Error indicators of analyzer such as CDR Unlock, Data Loss, Symbol Loss and Sync Loss (indicated by red LED).
- Error indicator for the current GUI state. When the current GUI is stopped, the respective indicator turns red.
- Calculated BER
- Alignment BER Threshold button to start BER threshold auto alignment.

The Status Indicator window always appears whenever you launch the M8070B user interface. However, you can open/close this window by clicking on the Status Indicator button, present on the status bar.
Logger Window

The Logger window displays errors and warnings messages along with their respective descriptions, applications from where they are generated and their time stamps.

The Logger window always appears whenever you launch the M8070B user interface. However, you can open/close this window by clicking on the Logger button, present on the status bar.

The Logger window allows you to:

- **Message Selection** - Use this option to choose whether you want to view errors, warnings or information message.
- **Copy** - Use this option to copy a message. You need to select a message in order to enable copy feature.
- **Select All** - Use this option to select all messages. It also enables copying all messages.
- **Clear Messages** - Use this option to delete all messages.
- **Auto Scroll** - Use this option to enable/disable auto scroll option. When the Auto Scroll option is enabled, it will automatically scroll you to the new message without using the scroll bar.
- **Open On Message** - Turn this button OFF if you don’t want the Logger window to automatically pop-up whenever a message is received.
- **Column Option** - Use this button to filter the messages either from Log From column or Date and Time column.
- **Search Messages** - Use this option to search messages by providing an input in the Search Messages search box.
Link Training Log Window

The Link Training Log window displays the logs for link training PCIe 3.0. You can open/close the Link Training Log window by clicking on the Link Training Log button present in the status bar. The Link Training Log button with orange background indicates an update or new entry in the link training log.

The following figure shows the Link Training Log window:

The Link Training Log window provides the following options:

- **Export Log** - Click the Export Log button to save the link training log.
- **Clear Logs** - Click the Clear Logs button to delete all link training logs.

For more details on link training, refer to Interactive Link Training on page 466.
Other GUI Features

Following are the GUI elements that make the M8070B user interface interactive.

**Tooltip**

The tooltip is a small pop-up window that concisely describes the object being pointed to, such as descriptions of toolbar controls, icons, graphics, links, menu items and taskbar buttons.

The following example shows the tooltip providing a description of toolbar buttons.

Here is another example where the tooltip provides information to the user on the minimum and maximum values the parameter can hold.

**Toggle Button**

The toggle button allows you to toggle between the two features. For example, in the following figure, we are using the toggle button to either expand or collapse the parameter list.
ON/OFF Switch

The ON/OFF switch enables or disables a given feature.

The following figure shows how a ON/OFF switch is used to turn the state feature ON.

![Output State Switch](image)

However, at some instances in the GUI, the ON/OFF switch will be enabled when you select the corresponding check box.

Execute Button

The **Execute** button allows you to perform an activity, once you click on it.

The following figure shows an **Execute** button that is used to perform pattern synchronization.

![Execute Button](image)

Drop-Down List

The drop-down list allows you to choose either one or sometimes multiple selections from the provided list.

The following shows the drop-down list to choose the **Re-Sync** mode.

![Drop-Down List](image)
Numeric Entries

Most numeric entries have a pre-defined maximum, minimum, and default value displayed in their corresponding pop-up menu.

Numeric values in numeric entries can be changed using the on-screen numeric keypad. For details, refer On-Screen Numeric Keypad on page 115.

Window Option

The window options allow you to float or dock anywhere in the application window. It provides quick access to logically grouped features from one location. For example, you can select and generate various layouts from the single window.

You can move a window anywhere on the screen or to a different monitor. You can also use the auto-hide feature of the windows to show or hide them on the desktop. You can also close the floating windows.

Auto Hide Feature

The automatic hiding functionality gives you the ability to imitate the behavior of the dock windows in the M8070B user interface. When it’s enabled for a dock panel, this panel is automatically hidden when the mouse pointer leaves its area. Dock panels are hidden at the nearest form's edge. For example, if a panel is docked to the right edge of the form, it will be hidden at the right edge.

End-users can enable the automatic hiding functionality by clicking the auto hide button displayed within the panel's caption.
The image below illustrates how the automatic hiding functionality can be enabled and how to show the hidden dock panel.

**Copying Parameter Window**

The copying feature creates a replica of parameters window to enhance the usability. It allows you to work on two different instances of the application. The changes you make in one window display immediately in the other window.

The following figure shows the copied parameters window.
Once copied and then enabling the auto hide feature, the cloned parameters window is docked to the right edge of the main user interface. The copied parameters window pops up once you click on it. The following figure shows the copied parameters window docked to the right edge of the main user interface.

On-Screen Numeric Keypad

The on-screen numeric keypad makes it easier to enter the numbers, units, etc., specially if you are using a touchscreen monitor. The on-screen numeric keypad pops up whenever you tap mouse pointer or touch (in case of touchscreen) in a text field or other area where user inputs are required.

**NOTE**

Remember to unselect the **Disable Keypad** option in the **Settings** window in order to enable the on-screen numeric keypad. For details, refer to **Settings Window** on page 535.

The following screen shows how to use an on-screen numeric keypad to provide a value to a parameter.
The on-screen numeric keypad contains the following buttons:

![Amplitude keypad](image)

Table 43  On-screen numeric keypad

<table>
<thead>
<tr>
<th>Button</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 8 9</td>
<td>Number Buttons</td>
<td>Press these buttons to enter a numeric value. The acceptable range of a parameter is shown at the top of the keypad.</td>
</tr>
<tr>
<td>4 5 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 2 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Decimal Button</td>
<td>Press this button to enter a decimal numeric value.</td>
</tr>
<tr>
<td>±</td>
<td>Function Button</td>
<td>Press this button to toggle between the addition (+) and subtraction (-) function.</td>
</tr>
<tr>
<td></td>
<td>UP/DOWN Button</td>
<td>Press these buttons to increase or decrease the numeric values, respectively.</td>
</tr>
<tr>
<td>Button</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Backspace Button</td>
<td>Press this button to delete</td>
<td>any character before the current position of the pointer.</td>
</tr>
<tr>
<td>LEFT/RIGHT Button</td>
<td>Press these buttons to move</td>
<td>the pointer one position left or right, respectively.</td>
</tr>
<tr>
<td>Exponent Button</td>
<td>Press this button to enter</td>
<td>exponents.</td>
</tr>
<tr>
<td>Enter Button</td>
<td>Press this button to apply</td>
<td>the value.</td>
</tr>
<tr>
<td>mV Button</td>
<td>Press this button to assign</td>
<td>units to the numeric value. Please note that the units may change depending</td>
</tr>
<tr>
<td></td>
<td>on the parameter.</td>
<td></td>
</tr>
<tr>
<td>Clear Field Button</td>
<td>Press this button to clear</td>
<td>the text field.</td>
</tr>
<tr>
<td>Minimum/Default/Maximum Button</td>
<td>Press this button to insert either minimum, or default, or maximum numeric value of the parameter.</td>
<td></td>
</tr>
</tbody>
</table>
Recall/Save Instrument State

Recall Instrument State

To recall an instrument state, do the following:

- Go to **File** menu and then click **Recall Instrument State**... The **Recall Instrument State** dialog will appear as shown in the following figure.

1. Select the folder (User or Factory) to view the files.
2. Select the file which is to be recalled.
3. Click **Recall**.
4. To rename a file, select the file and click **Rename**. The filename will become editable.
5. To delete a file, select the file and click **Delete**.
6. To add new folder, select location you want to create your folder and then click **New Folder**.
7. To rename a folder, select the folder and click **Rename**. The folder name will become editable.
8. To delete a folder, select the folder and click **Delete**.
Save Instrument State

To save an instrument state, do the following:

1. Go to **File** menu and then click **Save Instrument State...** The **Save Instrument State** dialog will appear as shown in the following figure.

![Save Instrument State dialog](image)

2. Enter a file name and click **Save**. The current settings will be saved under the filename.

3. To rename a file, select the file and click **Rename**. The filename will become editable.

4. To delete a file, select the file and click **Delete**.

5. To add new folder, select location you want to create your folder and then click **New Folder**.

6. To rename a folder, select the folder and click **Rename**. The folder name will become editable.

7. To delete a folder, select the folder and click **Delete**.
4 User Interface – M8070B Display Views

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Overview

The M8070B system software provides the following types of views:

- Module View
- System View
- Impairment Setup View
- Group View
- Setup View

In addition, on installing the Advanced Measurement Package, the following instruments can be controlled from M8070B System Software:

- N1076A/77A
- N1076B/78A
- Real-Time Oscilloscope

Description on the Advanced Measurement Package and steps to control the above instruments are explained in the M8000 Series Advanced Measurement Package User Guide.

**NOTE**

Please note that the Advanced Measurement Package requires license for its activation. For details on license, see M8070B Plugin Licenses on page 560.
Module View

The **Module View** is a graphical representation of the input/output ports that are present on the front panel of the modules, configured into the M8020A/M8030A/M8040A. The M8020A/M8030A supports the M8041A (8.5/16G Generator, Analyzer, Clock Module), M8051A (Generator-Analyzer), M8061A (32 Gb/s Multiplexer with De-emphasis) and M8062A modules that are installed into an Keysight M9505A 5-slot AXIe chassis. The M8040A supports the M8045A and M8046A modules that are installed into an Keysight M9505A 5-slot AXIe chassis. These modules have a different set of input/output ports depending upon their functionality e.g. generator, analyzer or clock. Each module consists of two channels (channel 1 and channel 2) depending upon the licenses, you have ordered. Each channel contains Data Out (Generator) and Data In (Analyzer) ports.

The modules are identified as M1, M2, M3 and so on in the GUI.

You can use the **Module View** to configure the properties of a single port or a group (combination of multiple ports). For details, refer to **Group View** on page 182.

**How to Launch Module View**

The **Module View** is launched by-default whenever you launch the M8070B user interface. However, if it is not available or is closed, you still can launch it.

To do so:

- Go to the **Menu Bar > System** and then select **Module View**.

The following figure shows an example of **Module View** when M8041A (M1) and M8051A (M2) modules are connected:
The left side shows the connected modules and the right side shows the Parameters window. Each module has input and output ports which can be configured through the Parameters window. For details on inputs and output ports, refer to Input and Output Ports on page 126. When you click on the port, the respective configurable parameters are displayed in the Parameters window. For details, refer to Parameters Window on page 133.
The following figure shows an example of **Module View** when M8041A (M1), M8051A (M2) and M8061A(M3) modules are connected:
The following figure shows an example of **Module View** when M8045A (M1) and M8046A (M2) modules are connected:

**Input and Output Ports**

**M8041A and M8051A Modules**

The M8041A (8.5/16G Generator, Analyzer, Clock Module) and M8051A (Generator-Analyzer) modules can have the following input and output ports:

- **Clock Gen**: Clock can be generated from the internal oscillator or an external source.
- **Data Out**: Data Out acts as the output port for the Generator which may be connected to the DUT. The data outputs serve as device stimuli and can be set up so that they are compatible with a variety of logic families.
- **Data In**: Data In acts as the input port for the Analyzer. This port is connected to the data signal which is the output of the DUT. Here the signal received and the signal generated internally is compared for calculating the bit error ratio.
• **Ref Clk Out**: The reference clock output is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment (SMA, female).

• **Clock Out**: The clock out port serves as frequency (bit rate) references. If we want to operate the external device at the system clock frequency then the device operating frequency can be set up using the clock out.

• **Trig Out**: Trig Out serves as an output port of the Generator. It allows you to connect a trigger for another device which can be used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment.

• **Sys Out A/Sys Out B**: System level control outputs used to signal events to the DUT or external instruments.

• **Ctrl Out A**: The module has one control output at the front panel with the following selectable functionality of Error Output.

• **Sys In A/Sys In B**: System level control inputs used to generate sequencer events.

• **Ctrl In A/Ctrl In B**: The M8041A and M8051A modules has two control inputs at the front panel each with the following selectable functionality of Error Add Input, Output Blanking, Electrical Idle and Gating Input.

### M8061A Module

The M8061A (32 Gb/s Multiplexer with De-emphasis) module has the following input and output ports:

• **Data In**: The M8061A has two Data In ports; Data In 1 and Data In 2 which are used to receive data from M8041A.

• **Data Out**: The M8061A Data Out port is used to provide the signals to DUT.

• **Elect Idle In**: This port is used to enable/disable the output signal by an external control signal. If the input level is above the threshold level the module enters electrical idle.
M8061A Configuration

The **M8061A Configuration** dialog provides configuration settings for M8061A. To open the **M8061A Configuration** dialog:

- Go to **Menu Bar > System** and then click **Module View**.
- Locate the **M8061A** module.
- Click **Configuration...** button.

The **M8061A Configuration** dialog will appear as shown in the following figure:

This dialog provides the following setting options:

- **Integration Mode**: Allows you to select the integration mode. The default mode is **Standalone** Mode. The other modes you can select are **Mux Only** mode, **Demux Only** mode and **Mux and Demux** mode.
• **Data Module**: Allows you to specify the data module to which the M8061A module is connected.

• **Demux Visa Resource**: Allows you to provide the visa resource string for N4877A. This is required to connect N4877A instrument with M8020A.

In addition, this dialog displays the connection diagram and connection instructions for each mode.

• Click **Apply**. Depending upon the configuration settings, the ports which in which settings can be done do not you will see the changes in the **Module View**. Some ports that are used by the data module and M8061A modules will be disabled. For the block diagram representation and interactively modify the settings of the currently mode, switch to **System View**. For details, refer System View with M8061A Integration on page 159.

**M8062A Module**

The M8062A (32Gb/s Front-end for J-BERT M8020A High-Performance BERT) module has the following ports on its front panel:

**On Pattern Generator Side**

• **Data In 1 and Data In 2 (Half Rate)** - Single-ended, half-rate data inputs from the M8041A module (3.5 mm, female).

• **Data Out and /Data Out** - Differential or single-ended, full-rate data output to the device under test. Unused outputs must be terminated into 50Ω. (2.4 mm, female).

• **DMI In** - Differential Mode Interference input. Applies a single-ended, external interference source differentially to the data output (SMA, female).

• **CMI In** - Common Mode Interference input. Applies a single-ended, external interference source to both the normal and complement data output signals (SMA, female).

• **Clk Out** - Half-rate Pattern Generator clock output. Carries the same jitter as the full-rate data output.

• **Clk In** - Pattern Generator clock input (half-rate). Connect to clock output of M8041A.

• **Aux Clk In** - Alternate Pattern Generator clock input (half-rate). Typically unused.

• **Electrical Idle In** - This input is used to enable/disable the output signal by an external control signal. If the input level is above the threshold level the module enters electrical idle. Normal operation resumes when the input level is below the threshold (SMA, female).
On Analyzer Side

- **Data In and /Data In** - Differential or single-ended, full-rate data input from the device under test. Unused input should be terminated into 50 Ω. (2.4 mm, female). These ports are AC coupled.

- **Data Out 1 and Data Out 2** - Single-ended, half-rate data outputs to the M8041A module (3.5 mm, female).

- **Clk Out** - Half-rate Error Analyzer clock output, synchronous with analyzer sampling.

- **Clk In** - Half-rate, Error Analyzer clock input. Allows external clocking of the Error Analyzer.

### M8062A Configuration

The **M8062A Configuration** dialog provides configuration settings for M8062A. To open the **M8062A Configuration** dialog:

- Go to **Menu Bar > System** and then click **Module View**.
- Locate the M8062A module.
- Click **Configuration...** button.

The **M8062A Configuration** dialog will appear as shown in the following figure:
This dialog displays the connection diagram and connection instructions.

- **Click Enable.** In the 32G mode, access to some M8041A user controls are disabled to facilitate software control of this configuration. For the block diagram representation and to interactively modify the settings of the currently 32G mode, switch to **System View**. For details, refer **System View with M8062A Integration** on page 166.

### M8045A Module

The M8045A module has the following ports on its front panel:

- **Remote Head - P and N Ports** - The P and N ports of each channel must be connected to the M8057A/B.

- **Clk Out1 and Clk Out 2** - These are the Clk Out ports of channel 1 and 2, respectively. It can generate either a Clean Clk or all timing impairments like Data Out.

- **Ref Clock In** - The Ref Clk In input can be used as reference frequency or as external system frequency directly for the instrument. An external provided signal can be measured at that input. This input is tightly involved in the system frequency generation.
• **Ref Clock Out** - The Ref Clk Out is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment.

• **Clock Out and Clock Out** - The differential clock output serve as frequency (bit rate) reference and can be set up so that they are compatible with a variety of logic families. With respect to Clock Out, Clock Out has inverted logic.

• **Trigger Out and Trigger Out** - This port allows you to trigger another device (for example, an oscilloscope) and can be set up so that they are compatible with a variety of logic families. Trigger Out has more modes, e.g. sub rate clock to be used as ref clock for a DUT. With respect to Trigger Out, Trigger Out has inverted logic.

• **Sys Out A/B** - The system level control outputs used to trigger events to the DUT or external instruments.

• **Ctrl Out A** - The control output port provides the Error Output functionality.

### Show Module Information

You can get the module information that is connected to the M8020A by clicking the icon present at the right side of each module. The module information will be shown as depicted in the following figure:

It provides the following information about the module:

- **Address** - Address of module, e.g. USB-PXI0::11::0::INSTR
- **Product Number** - Product no. of the module, e.g. M8041A
- **Serial Number** - Serial no. of module, e.g. DE53C00061
- **Hardware Revision** - Hardware revision of module, e.g. 0
Selecting Single/Multiple Ports

You can select either single or multiple ports by pressing the toggle button, available on the top of the main window. It provides the following modes selection:

- **Single Selection Mode** - allows you to select only one port at a time from the connected modules.

- **Multiple Selection Mode** - allows you to select multiple ports from the connected modules.

Parameters Window

The **Parameters** window displays the functional blocks of the selected port/port groups. Each functional block has a set of parameters. The **Parameters** window also allows you to set the parameters of the selected port/port groups.

If you try to set a parameter which conflicts with other parameter or in other words is dependent on other parameter, a **Auto Correct Confirmation** dialog appears. For details, see **Auto Correction Confirmation Dialog** on page 137.

The **Parameters** window is shown in the following figure:
The **Parameters** window has the following sections:
- Tool bar
- Display Grid
- Parameters Description Pane

The **Parameters** window tool bar includes the following icons:

- ![Expand/Collapse All Group](Image)
  - Click this icon to expand or collapse the functional blocks.

- ![Show Search Option](Image)
  - Allows you to filter and customize your results by using the following options:
    - By Location
    - By Functional Block
    - By Property

- ![Copying Parameter Window](Image)
  - Creates a replica of **Parameters** window to enhance the usability. It allows you to work on two different instances of the application. The changes you make in one window display immediately in the other window. The icon present on the copied parameter window loads all properties of the module. The following figure shows the copied **Parameters** window.

Once copied and then enabling the auto hide feature, the copied parameters window is docked to the right edge of the main user interface. The copied parameters window pops up once you click on it.
The following figure shows the copied parameters window docked to the right edge of the main user interface.

- **Display Grid**: Displays the parameters of the selected port/port groups within a grid. The left column contains the parameter names; the right column contains the parameter values. In addition, it also allows you to set the parameters of the selected port/port groups. The naming convention used for the port/port group is explained with the help of following example:
  
  M1.DataIn1

  Where,
  
  - M1 stands for Module1
  - DataIn stands for DataIn port
  - 1 for channel 1

  The functional blocks use the different color schemes to represent different channels. You can set the color schemes of each channel from the Setting window. For details, refer to [Settings Window](#) on page 535.

- **Parameter Description Pane**: Provides the description and related SCPI of the currently selected parameter.
  
  The following figure shows the Parameter Description Pane providing the description and the related SCPI when the line coding parameter is selected.
**Copy-Paste Parameters Settings**: The Parameter Window allows you to copy all parameter’s settings of one location to the another similar location within the same module. This helps to keep the similar parameter settings for same locations across different channels. For example, if you want to copy the parameter’s setting of DataOut of channel 1 to DataOut of channel 2, just right-click on DataOut of channel 1 and select **Copy** and then right-click on DataOut of channel 2 and select **Paste**.

The following figure illustrates how copy-paste of one location to another similar location within a module is done:
Auto Correction Confirmation Dialog

There are several parameters in the M8070B GUI which are interdependent on the settings of other parameters. For details of these parameters, refer to Table 44 on page 137 and Table 45 on page 145.

An Auto Correct Confirmation dialog appears if you try to set a parameter which conflicts with other parameter or in other words is dependent on the settings of other parameter. This dialog display the conflicts encountered and also provides the recommended setting to overcome those conflicts. If you click Apply button, the recommended settings will be applied on the M8070B GUI. However, if you click Discard button, the previous settings will be applied. The following figure shows an Auto Correct Confirmation dialog which is displayed when a user tries to set a ClkGen frequency and it conflicts with ClkOut Output Timing Divider.

![Auto Correct Confirmation Dialog](image)

Dependent Parameters

There are several parameters in the M8070B GUI which are interdependent on the settings of other parameters. Refer to Table 44 on page 137 and Table 45 on page 145 for details of these parameters. For details on the related/dependent SCPIs of these parameters, please refer to M8000 Series Programming Guide.

Table 44  M8020A/M8030A Dependent Parameters
<table>
<thead>
<tr>
<th>Functional block / Identifier Location</th>
<th>Dependent Parameters</th>
<th>Description</th>
<th>Related /Dependent SCPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>Depends on amplitude and offset value</td>
<td><em>=SOURce:VOLTage:HIGH :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet</em></td>
<td></td>
</tr>
<tr>
<td>Low</td>
<td>Depends on amplitude and offset value</td>
<td><em>=SOURce:VOLTage:LOW :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet</em></td>
<td></td>
</tr>
<tr>
<td>Offset</td>
<td>Depends on termination voltage</td>
<td><em>=SOURce:VOLTage:OFFSet :OUTPut:TVOLtage</em></td>
<td></td>
</tr>
<tr>
<td>Amplitude Range</td>
<td>DataOut maximum amplitude will become limited to the selected amplitude range value</td>
<td><em>=SOURce:VOLTage:AMPLitude :SOURce:VOLTage:RANGe:AUTO :SOURce:VOLTage:RANGe:SELect :OUTPut:STATe</em></td>
<td></td>
</tr>
<tr>
<td>Coupling</td>
<td>Selecting incorrect coupling enables output protection, and as a result DataOut state could not be enabled</td>
<td><em>=OUTPut:STATe :OUTPut:COUPling</em></td>
<td></td>
</tr>
<tr>
<td>Termination Model</td>
<td>Only available when coupling is selected as DC</td>
<td><em>=OUTPut:COUPling :OUTPut:TCONfig</em></td>
<td></td>
</tr>
<tr>
<td>Termination Voltage</td>
<td>Available only if coupling is selected as DC and termination model is selected as unbalanced</td>
<td><em>=OUTPut:COUPling :OUTPut:TCONfig :OUTPut:TVOLtage</em></td>
<td></td>
</tr>
<tr>
<td>CMI State</td>
<td>CMI value depends only if CMI state is enabled</td>
<td><em>=SOURce:INTerference:LEVel:CMODe:STATe :SOURce:INTerference:LEVel:CMODe:AMPLitude</em></td>
<td></td>
</tr>
<tr>
<td>CMI Amplitude</td>
<td>DataOut maximum amplitude will be limited to 900mV if CMI state is enabled</td>
<td><em>=SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:CMODe:STATe :SOURce:INTerference:LEVel:CMODe:AMPLitude :OUTPut:STATe</em></td>
<td></td>
</tr>
<tr>
<td>DMI State</td>
<td>Depends on DataOut Amplitude maximum value</td>
<td><em>=SOURce:INTerference:LEVel:DMODe:STATe :SOURce:INTerference:LEVel:DMODe:AMPLitude</em></td>
<td></td>
</tr>
<tr>
<td>DMI Amplitude</td>
<td>On applying DMI amplitude as max (360mV) then maximum value of DataOut1 Amplitude will become 840mV</td>
<td><em>=SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:DMODe:STATe :SOURce:INTerference:LEVel:DMODe:AMPLitude :OUTPut:STATe</em></td>
<td></td>
</tr>
</tbody>
</table>
### LF Jitter

**M1.DataOut1**

#### RJ State

Value doesn’t applicable if state is Off

```
:SOURce:JITTER:LFRequency:PERiodic:STATe
```

#### RJ Amplitude

RJ amplitude depends on RJ frequency, rSSC amplitude, rSSC state and rSSC frequency

```
:SOURce:JITTER:LFRequency:PERiodic:AMPLitude
:SOURce:JITTER:LFRequency:PERiodic:FREQuency
:SOURce:JITTER:LFRequency:RSSClocking:STATe
:SOURce:JITTER:LFRequency:RSSClocking:AMPLitud
:SOURce:JITTER:LFRequency:RSSClocking:FREQuenc
```

#### RJ Frequency

RJ frequency depends on RJ amplitude, rSSC amplitude, rSSC state and rSSC frequency

```
:SOURce:JITTER:LFRequency:PERiodic:STATe
:SOURce:JITTER:LFRequency:PERiodic:AMPLitude
:SOURce:JITTER:LFRequency:PERiodic:FREQuency
:SOURce:JITTER:LFRequency:RSSClocking:STATe
:SOURce:JITTER:LFRequency:RSSClocking:AMPLitud
:SOURce:JITTER:LFRequency:RSSClocking:FREQuenc
```

#### rSSC State

Value doesn’t applicable if state is Off

```
:SOURce:JITTER:LFRequency:RSSClocking:STATe
```

#### rSSC Amplitude

rSSC amplitude depends on rSSC frequency, RJ amplitude, RJ state and RJ frequency

```
:SOURce:JITTER:LFRequency:PERiodic:STATe
:SOURce:JITTER:LFRequency:PERiodic:AMPLitude
:SOURce:JITTER:LFRequency:PERiodic:FREQuency
:SOURce:JITTER:LFRequency:RSSClocking:STATe
:SOURce:JITTER:LFRequency:RSSClocking:AMPLitud
:SOURce:JITTER:LFRequency:RSSClocking:FREQuenc
```

#### rSSC Frequency

rSSC frequency depends on rSSC amplitude, RJ amplitude, RJ state and RJ frequency

```
:SOURce:JITTER:LFRequency:PERiodic:STATe
:SOURce:JITTER:LFRequency:PERiodic:AMPLitude
:SOURce:JITTER:LFRequency:PERiodic:FREQuency
:SOURce:JITTER:LFRequency:RSSClocking:STATe
:SOURce:JITTER:LFRequency:RSSClocking:AMPLitud
:SOURce:JITTER:LFRequency:RSSClocking:FREQuenc
```

#### Unit

If unit is selected as ‘sec’, the jitter amplitude min/max values also depends on Data rate (synthesizer frequency)

```
:SOURce:JITTER:LFRequency:UNIT
:SOURce:FREQuency
```
### HF Jitter M1.DataOut1 PJ1 State

Value doesn't applicable if state is Off

- :SOURce:JITTer:HFRequency:PERiodic1:STATe

- PJ1 Amplitude
  - "Depends on PJ2 amplitude, BUJ amplitude, RJ amplitude, sRJ amp1 and sRJ amp2 (User can choose either sRJ Or combination of BUJ and RJ)"
  - :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude
  - :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude
  - :SOURce:JITTer:HFRequency:RANDom:AMPLitude
  - :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1
  - :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2

- R2 State
  - Value doesn't applicable if state is Off
  - :SOURce:JITTer:HFRequency:PERiodic2:STATe

- R2 Amplitude
  - "Depends on PJ1 amplitude, BUJ amplitude, RJ amplitude, sRJ amp1 and sRJ amp2 (User can choose either sRJ Or combination of BUJ and RJ)"
  - :SOURce:JITTer:HFRequency:PERiodic1:AMPLitude
  - :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude
  - :SOURce:JITTer:HFRequency:RANDom:AMPLitude
  - :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1
  - :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2

- BUJ State
  - "Value doesn't applicable if state is Off Also depends on sRJ state"
  - :SOURce:JITTer:HFRequency:BUNCorrelate:STATe
  - :SOURce:JITTer:HFRequency:SPECtrally:STATe

- BUJ Amplitude
  - Depends on PJ1 amplitude, PJ2 amplitude, RJ amplitude, sRJ amp1 and sRJ amp2
  - :SOURce:JITTer:HFRequency:PERiodic1:AMPLitude
  - :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude
  - :SOURce:JITTer:HFRequency:RANDom:AMPLitude
  - :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1
  - :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2

- RJ State
  - "Value doesn't applicable if state is Off Also depends on sRJ state"
  - :SOURce:JITTer:HFRequency:RANDom:STATe
  - :SOURce:JITTer:HFRequency:SPECtrally:STATe

---

**Data rate (Synthesizer frequency)**

If unit is selected as 'sec', the jitter amplitude min/ max values also depends on Data rate (synthesizer frequency)

*:SOURce:JITTer:LFRequency:UNIT
:SOURce:FREQuency"
### RJ Amplitude
- Depends on PJ1 amplitude, PJ2 amplitude, BUJ amplitude, sRJ amp1, and sRJ amp2
- `*SOURce:JITTer:HFRequency:PERiodic1:AMPLitude`
- `*SOURce:JITTer:HFRequency:PERiodic2:AMPLitude`
- `*SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude`
- `*SOURce:JITTer:HFRequency:SPECTrally:AMPLitude1`
- `*SOURce:JITTer:HFRequency:SPECTrally:AMPLitude2`

### sRJ State
- Value doesn't applicable if state is Off
- Also depends on RJ and BUJ state
- `*SOURce:JITTer:HFRequency:SPECTrally:STATe`
- `*SOURce:JITTer:HFRequency:RANDom:STATe`
- `*SOURce:JITTer:HFRequency:BUNCorrelate:STATe`

### sRJ Amplitude 1 (RMS) LF
- Depends on PJ1 amplitude, PJ2 amplitude, BUJ amplitude, RJ amp, and sRJ amp2
- `*SOURce:JITTer:HFRequency:PERiodic1:AMPLitude`
- `*SOURce:JITTer:HFRequency:PERiodic2:AMPLitude`
- `*SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude`
- `*SOURce:JITTer:HFRequency:SPECTrally:AMPLitude1`
- `*SOURce:JITTer:HFRequency:SPECTrally:AMPLitude2`

### sRJ Amplitude 2 (RMS) HF
- Depends on PJ1 amplitude, PJ2 amplitude, BUJ amplitude, RJ amp, and sRJ amp1
- `*SOURce:JITTer:HFRequency:PERiodic1:AMPLitude`
- `*SOURce:JITTer:HFRequency:PERiodic2:AMPLitude`
- `*SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude`
- `*SOURce:JITTer:HFRequency:SPECTrally:AMPLitude1`
- `*SOURce:JITTer:HFRequency:SPECTrally:AMPLitude2`

### sRJ State
- BUJ State (Data Out)
  - If sRJ is ON, then BUJ state cannot be enabled
  - `*SOURce:JITTer:HFRequency:SPECTrally:STATe`
  - `*SOURce:JITTer:HFRequency:BUNCorrelate:STATe`

### RJ State
- BUJ State (Data Out)
  - If sRJ is ON, then RJ state cannot be enabled
  - `*SOURce:JITTer:HFRequency:SPECTrally:STATe`
  - `*SOURce:JITTer:HFRequency:RANDom:STATe`

### BUJ State
- RJ State (Clock Out)
  - If sRJ is ON, then BUJ state cannot be enabled
  - `*SOURce:JITTer:HFRequency:SPECTrally:STATe`
  - `*SOURce:JITTer:HFRequency:BUNCorrelate:STATe`

### RJ State
- BUJ State (Data Out)
  - If BUJ state is ON, then DataOut sRJ cannot be enabled
  - `*SOURce:JITTer:HFRequency:SPECTrally:STATe`
  - `*SOURce:JITTer:HFRequency:RANDom:STATe`

### sRJ State
- RJ State (Clock Out)
  - If RJ state is ON, then ClockOut sRJ cannot be enabled
  - `*SOURce:JITTer:HFRequency:SPECTrally:STATe`
  - `*SOURce:JITTer:HFRequency:RANDom:STATe`
<table>
<thead>
<tr>
<th>Functional block / Parameter</th>
<th>Identifier Location</th>
<th>Dependent Parameters</th>
<th>Description</th>
<th>Related /Dependent SCPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>sRJ State (Data Out)</td>
<td>M1.DataOut1</td>
<td>RJ State (Data Out)</td>
<td>If sRJ state is ON, then DataOut sRJ cannot be enabled</td>
<td><em>SOURce:JITTER:HFRequency:RANDom:STATe ; SOURce:JITTER:HFRequency:SPECtrally:STATe</em></td>
</tr>
<tr>
<td>sRJ Low Pass Filter</td>
<td>M1.DataOut1</td>
<td>RJ State (Data Out)</td>
<td>Depends on Data Rate (Synthesizer frequency)</td>
<td>Can only be selected if Data Rate is above 7.5 GHz</td>
</tr>
<tr>
<td>Jitter Sweep State</td>
<td>M1.DataOut1</td>
<td>RJ State (Data Out)</td>
<td>If Jitter Sweep state is ON, then DataOut RJ cannot be enabled</td>
<td><em>SOURce:JITTER:SWEep:STATe ; SOURce:JITTER:HFRequency:RANDom:STATe</em></td>
</tr>
<tr>
<td>Jitter Sweep Profile</td>
<td>M1.DataOut1</td>
<td>RJ State (Clock Out)</td>
<td>If Jitter Sweep state is ON, then ClockOut RJ cannot be enabled</td>
<td><em>SOURce:JITTER:SWEep:STATe ; SOURce:JITTER:HFRequency:PERiodic:STATe</em></td>
</tr>
<tr>
<td>Jitter Sweep Step Distance</td>
<td>M1.DataOut1</td>
<td>RJ State (Clock Out)</td>
<td>If Jitter Sweep state is ON, then ClockOut RJ cannot be enabled</td>
<td><em>SOURce:JITTER:SWEep:STATe ; SOURce:JITTER:HFRequency:PERiodic:STATe</em></td>
</tr>
<tr>
<td>Jitter Sweep Step Distance</td>
<td>M1.DataOut1</td>
<td>Jitter sweep mode</td>
<td>Jitter sweep step distance parameter is re-programmable only if Mode is selected as Variable amplitude</td>
<td><em>SOURce:JITTER:SWEep:STATe ; SOURce:JITTER:SWEep:AMPLitude:MODE ; SOURce:JITTER:SWEep:STEP:DISTance</em></td>
</tr>
<tr>
<td>Functional block / Parameter</td>
<td>Identifier Location</td>
<td>Dependent Parameters</td>
<td>Description</td>
<td>Related /Dependent SCPI</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>---------------------</td>
<td>----------------------</td>
<td>-------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>CMI Amplitude</td>
<td>M1.DataOut1</td>
<td>CMI State</td>
<td>Value doesn’t applicable if state is Off</td>
<td><em>:SOURce:VOLTage:AMPLitude :SOURce:INterference:LEVel:CMODe:STATe :SOURce:INterference:LEVel:CMODe:AMPLitude</em></td>
</tr>
<tr>
<td>DMI Amplitude</td>
<td>M1.DataOut1</td>
<td>DMI State</td>
<td>Value doesn’t applicable if state is Off</td>
<td><em>:SOURce:VOLTage:AMPLitude :SOURce:INterference:LEVel:DMODe:STATe :SOURce:INterference:LEVel:DMODe:AMPLitude</em></td>
</tr>
<tr>
<td>Error Insertion Ratio</td>
<td>M1.DataOut1</td>
<td>Error Insertion Mode</td>
<td>Error ratio of 1E-1 or 1E-2 are selectable only if error insertion mode is selected as Variable spacing</td>
<td><em>:OUTPut:EINSertion:MODE :OUTPut:EINSertion:RATio</em></td>
</tr>
<tr>
<td>Inter-Symbol Interference Mode</td>
<td>M1.DataOut1</td>
<td></td>
<td>ISI mode as Two-Point only available when Preset is selected as Custom</td>
<td><em>:SOURce:INterference:ISYMbol:MODE :SOURce:INterference:ISYMbol:PRESet</em></td>
</tr>
<tr>
<td>De-emphasis Preset Register Number</td>
<td>M1.DataOut1</td>
<td>State of Preset Enable button</td>
<td>Re-programmable only if state of Preset Enable button is ON</td>
<td><em>:OUTPut:DEEmphasis:PRESet:ENABle :OUTPut:DEEmphasis:PRESet</em></td>
</tr>
<tr>
<td>Bit Recovery Mode State</td>
<td>M1.DataIn1</td>
<td>Depends on CDR State</td>
<td>BRM mode can only be enabled if CDR state is ON</td>
<td><em>:INPut:CDR:JTF:STATe :INPut:DATA:BRMode</em></td>
</tr>
<tr>
<td>Functional block / Parameter</td>
<td>Identifier Location</td>
<td>Dependent Parameters</td>
<td>Description</td>
<td>Related /Dependent SCPI</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>---------------------</td>
<td>---------------------</td>
<td>-------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>CDR State</td>
<td>M1.DataIn1</td>
<td>Depends on CDR Control type</td>
<td>If CDR control type is Sequence controlled, then CDR state will be controlled by Analyzer sequence block settings</td>
<td>:INPut:CDR:CTRL</td>
</tr>
<tr>
<td>CDR Loop Bandwidth</td>
<td>M1.DataIn1</td>
<td>Depends on Data Rate</td>
<td>Maximum value of CDR loop bandwidth depends on Data rate (Synthesizer frequency)</td>
<td>*.INPut:CDR:JTF:STATe :SOURce:FREQuency&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Depends on Loop Order</td>
<td>Depends on type of the selected loop order</td>
<td><em>.INPut:CDR:JTF:STATe :INPut:CDR:JTF:ORDer</em></td>
</tr>
<tr>
<td>Comparator Compare Mode</td>
<td>M1.DataIn1</td>
<td>Depends on Termination Configuration</td>
<td>Available only if Termination configuration is selected as Unbalanced</td>
<td>:INPut:TCONfig</td>
</tr>
<tr>
<td>Termination Voltage</td>
<td>M1.DataIn1</td>
<td>Depends on Termination Configuration</td>
<td>Available only if Termination configuration is selected as Unbalanced</td>
<td><em>.INPut:TCONfig :INPut:TVOLTage :INPut:CMODE</em></td>
</tr>
<tr>
<td>SSC Profile Shape</td>
<td>M1.ClkGen</td>
<td>Depends on SSC Profile</td>
<td>Available only if SSC profile is selected as Arbitrary</td>
<td><em>.SOURce:SSCLocking:STATe :SOURce:SSCLocking:PROFile :SOURce:SSCLocking:SHApe</em></td>
</tr>
<tr>
<td>Functional block / Parameter</td>
<td>Identifier Location</td>
<td>Dependent Parameters</td>
<td>Description</td>
<td>Related /Dependent SCP</td>
</tr>
<tr>
<td>------------------------------</td>
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<td>-------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>M8046A Follow Sys Clock Option</td>
<td></td>
<td></td>
<td>Depends on amplitude and offset value</td>
<td><em>:SOURce:VOLTage:HIGH :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet</em></td>
</tr>
<tr>
<td>Amplifier</td>
<td>M1.DataOut1</td>
<td>Amplitude</td>
<td>Depends on termination voltage and synthesizer frequency</td>
<td><em>:SOURce:VOLTage:AMPLitude :OUTPut:TVOLtage :SOURce:FREQuency</em></td>
</tr>
<tr>
<td>High</td>
<td></td>
<td></td>
<td>Depends on amplitude and offset</td>
<td><em>:SOURce:VOLTage:HIGH :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet</em></td>
</tr>
<tr>
<td>Low</td>
<td></td>
<td></td>
<td>Depends on amplitude and offset</td>
<td><em>:SOURce:VOLTage:LOW :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet</em></td>
</tr>
<tr>
<td>Offset</td>
<td></td>
<td></td>
<td>Depends on termination voltage</td>
<td><em>:SOURce:VOLTage:OFFSet :OUTPut:TVOLtage</em></td>
</tr>
<tr>
<td>Coupling</td>
<td></td>
<td></td>
<td>Selecting incorrect coupling enables output protection, and as a result DataOut state could not be enabled</td>
<td><em>:OUTPut:STATe :OUTPut:COUPling</em></td>
</tr>
<tr>
<td>Termination Model</td>
<td>Only available when coupling is selected as DC</td>
<td></td>
<td><em>:OUTPut:COUPling :OUTPut:TCONfig</em></td>
<td></td>
</tr>
<tr>
<td>Termination Voltage</td>
<td>Available only if coupling is selected as unbalanced</td>
<td></td>
<td><em>:OUTPut:COUPling :OUTPut:TCONfig :OUTPut:TVOLtage</em></td>
<td></td>
</tr>
<tr>
<td>Functional block / Parameter</td>
<td>Identifier Location</td>
<td>Dependent Parameters</td>
<td>Description</td>
<td>Related /Dependent SCP</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>---------------------</td>
<td>----------------------</td>
<td>-------------</td>
<td>------------------------</td>
</tr>
<tr>
<td>Clock Gen Frequency</td>
<td>M1.DataOut1</td>
<td>Automatic main cursor state</td>
<td>Re-programmable only if Automatic main cursor state is disabled</td>
<td>&quot;:OUTPut:DEEmphasis:CURSor:MAIN:AUTO :OUTPut:DEEmphasis:CURSor:MAGNitude2&quot;</td>
</tr>
<tr>
<td>De-emphasis Co-efficient 2</td>
<td>M1.DataOut1</td>
<td>Depends on Coefficient 0, 1 and 3 state</td>
<td>De-emphasis coefficient values are interdependent and sum of all the cursors cannot be more than 1.0</td>
<td>&quot;:OUTPut:DEEmphasis:CURSor:MAIN:AUTO :OUTPut:DEEmphasis:CURSor:MAGNitude0 :OUTPut:DEEmphasis:CURSor:MAGNitude1 :OUTPut:DEEmphasis:CURSor:MAGNitude2 :OUTPut:DEEmphasis:CURSor:MAGNitude3&quot;</td>
</tr>
<tr>
<td>LF Jitter</td>
<td>M1.DataOut1</td>
<td>RJ State</td>
<td>Value doesn't applicable if state is Off</td>
<td>&quot;:SOURce:JITTer:LFRequency:PERiodic:STATe&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Unit</td>
<td>If unit is selected as sec, then amplitude min/max values will be expressed in sec</td>
<td>&quot;:SOURce:JITTer:LFRequency:UNIT :SOURce:FREQuency&quot;</td>
</tr>
<tr>
<td>HF Jitter</td>
<td>M1.DataOut1</td>
<td>RJ1 State</td>
<td>Value doesn't applicable if state is Off</td>
<td>&quot;:SOURce:JITTer:HFRequency:PERiodic1:STATe&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RJ2 State</td>
<td>Value doesn't applicable if state is Off</td>
<td>&quot;:SOURce:JITTer:HFRequency:PERiodic2:STATe&quot;</td>
</tr>
<tr>
<td>Functional block / Parameter</td>
<td>Identifier Location</td>
<td>Dependent Parameters</td>
<td>Description</td>
<td>Related / Dependent SCP</td>
</tr>
<tr>
<td>------------------------------</td>
<td>---------------------</td>
<td>----------------------</td>
<td>-------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>BUJ State</td>
<td></td>
<td></td>
<td>Value doesn't applicable if state is Off</td>
<td>:SOURce:JITTer:HFRequency:BUncorrelate:STATe</td>
</tr>
<tr>
<td>RJ State</td>
<td></td>
<td></td>
<td>Value doesn't applicable if state is Off</td>
<td>:SOURce:JITTer:HFRequency:RANDom:STATe</td>
</tr>
<tr>
<td>Error Insertion Ratio</td>
<td>M1.DataOut1</td>
<td>Error Insertion Mode</td>
<td>Error ratio of 1E-1 or 1E-2 are selectable only if error insertion mode is selected as Variable spacing</td>
<td>:OUTPut:EINSertion:MODE :OUTPut:EINSertion:RATio*</td>
</tr>
<tr>
<td>N8046A Clock</td>
<td>M2.DataIn</td>
<td>Clock Source</td>
<td>Some parameters only available if clock source is selected as CLK IN</td>
<td>:CLOCk:SOURce</td>
</tr>
<tr>
<td>Follow Sys Clock</td>
<td></td>
<td></td>
<td>Follow Sys Clk option only available if clock source is selected as CLK IN</td>
<td>:CLOCk:SOURce :CLOCk:TRACk:STATe*</td>
</tr>
<tr>
<td>Clk In Multiplier</td>
<td></td>
<td></td>
<td>Clk In multiplier value depends on Data rate and available only if clock source is selected as CLK IN</td>
<td>:CLOCk:SOURce :CLOCk:FREQuency:MULTiplier*</td>
</tr>
<tr>
<td>Clock Source as External Clock Recovery</td>
<td>M2.DataIn</td>
<td>Clock Source</td>
<td>Available only if FlexDCA is configured for M8070B and N1076A module is connected with the system running M8070B</td>
<td>:CLOCk:SOURce</td>
</tr>
<tr>
<td>Custom Symbol Mapping</td>
<td>M2.DataIn/ M1.DataOut1</td>
<td>Line Coding</td>
<td>Available only if Line coding is selected as PAM4 and Symbol mapping is selected as Custom</td>
<td>:DATA:LINecoding:VALue :DATA:LINecoding:PAM4:MAPPing :DATA:LINecoding:PAM4:SYMBol:LEVel1 :DATA:LINecoding:PAM4:SYMBol:LEVel2*</td>
</tr>
</tbody>
</table>
## Functional block / Parameter

<table>
<thead>
<tr>
<th>Identifier</th>
<th>Location</th>
<th>Dependent Parameters</th>
<th>Description</th>
<th>Related / Dependent SCP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper, Middle</td>
<td>M2.DataIn</td>
<td>Depends on Line Coding</td>
<td>Available only if Line coding is selected as PAM4</td>
<td>:DATA:LINecoding:VALue</td>
</tr>
<tr>
<td>and Lower</td>
<td></td>
<td></td>
<td></td>
<td>:DATA:LINecoding:PAM4:MAPPING</td>
</tr>
<tr>
<td>Thresholds</td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:VOLTage:PAM4:SYMBol:THReshold1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:VOLTage:PAM4:SYMBol:THReshold2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:VOLTage:PAM4:SYMBol:THReshold3</td>
</tr>
<tr>
<td>Alignment</td>
<td>M2.DataIn</td>
<td>Depends on Line Coding</td>
<td>Available only if Line coding is selected as PAM4 (Only Query Command)</td>
<td>:DATA:LINecoding:VALue</td>
</tr>
<tr>
<td>results for</td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:ALIGNment:EYE:RESult:PAM4:HEIGht1</td>
</tr>
<tr>
<td>Upper, Middle</td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:ALIGNment:EYE:RESult:PAM4:HEIGht2</td>
</tr>
<tr>
<td>and Lower Eye</td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:ALIGNment:EYE:RESult:PAM4:HEIGht3</td>
</tr>
<tr>
<td>Height</td>
<td></td>
<td></td>
<td></td>
<td>:DATA:LINecoding:VALue</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:ALIGNment:EYE:RESult:PAM4:THReshold1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:ALIGNment:EYE:RESult:PAM4:THReshold2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>:INPUT:ALIGNment:EYE:RESult:PAM4:THReshold3</td>
</tr>
<tr>
<td>PRBS Polynomial</td>
<td>Sequence Editor</td>
<td>Depends on Analyzer sequence</td>
<td>Not downloadable for Analyzer sequence for M8046A module</td>
<td>:DATA:SEQUence:VALue</td>
</tr>
<tr>
<td>as 2^7-1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbol Width</td>
<td>Sequence Editor</td>
<td>M8045A and M8046A only support Symbol Width as 1</td>
<td>Symbol width other that 1 are not supported on M8040A modules</td>
<td>:DATA:SEQUence:VALue</td>
</tr>
<tr>
<td>other than 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>for M8045A and</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M8046A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Branch condition</td>
<td>Sequence Editor</td>
<td>Branch condition as Break is not supported for Analyzer sequence</td>
<td>Branch condition as Break is not supported for Analyzer sequence</td>
<td>:DATA:SEQUence:VALue</td>
</tr>
<tr>
<td>as Break for</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M8046A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RJ Low Pass</td>
<td>M1.DataOut1</td>
<td>Depends on Data Rate (Synthesizer frequency)</td>
<td>Can only be selected is Data Rate is above 7.5 GHz</td>
<td>:SOURce:JITTer:HFRequency:RANDom:STATe</td>
</tr>
<tr>
<td>Filter as 1000</td>
<td></td>
<td></td>
<td></td>
<td>:SOURce:FREQuency</td>
</tr>
<tr>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
<td>:SOURce:JITTer:HFRequency:RANDom:FILTER:LPASs</td>
</tr>
</tbody>
</table>
Non-Configurable Parameters

The Table 46 on page 149 lists the M8040A parameters which are non-configurable (read-only/gray out/disabled) by default or become non-configurable while configuring other dependent parameters.

Table 46  M8040A Non-Configurable Parameters

<table>
<thead>
<tr>
<th>Functional block name</th>
<th>Parameters</th>
<th>Disabled parameters</th>
<th>Parameters that are non-configurable by default</th>
<th>Parameters that are non-configurable due to settings of other parameters</th>
</tr>
</thead>
</table>
| Clk Gen                | Synthesizer (Select Source as Direct) | • Frequency  
                         • Period | • In the Direct source mode, Frequency and Period will be in disabled state. | | |
|                        | Synthesizer (Select Source as Clock Multiplier) | • Frequency  
                         • Period | • In the Clock Multiplier mode, Frequency and Period will be in disabled state. | | |
|                        | SSC       | • Shape             | • The SSC Shape parameters (Open, Import, Export and Reset to Default) are disabled by default. These parameters are enabled when SSC Profile is selected as Arbitrary. | | |
| Data Out               | Line Coding (Select PAM) | • Symbol 0 Level  
                         • Symbol 3 Level | • In the PAM4 Line Coding, Symbol 0 Level and Symbol 3 Level are in disabled state by default. | | |
| Amplifier             |           | • Termination Voltage  
                         • Coupling  
                         • Termination Model | • In the DC Unbalanced mode, all these three parameters become disabled on turning ON the output state. | | |
| Amplifier             |           | • Termination Voltage  
                         • Coupling  
                         • Termination Model | • In the DC Balanced mode, on turning ON the output state, Coupling and Termination Model are disabled and Termination Voltage is not available for user. | | |
| Amplifier             |           | • High  
                         • Low  
                         • Offset  
                         • Termination Voltage  
                         • Termination Model | • On selecting Coupling as AC, High, Low and offset parameters are disabled. Also, Termination Voltage and Termination Model are unavailable in AC coupling. | | |
### De-Emphasis
- Coefficient 2 (Main)
- Output Swing
- Pre-cursor2
- Pre-cursor1
- Post-cursor1

In the De-Emphasis block, Coefficient 2 (Main), Output Swing, Pre-cursor2, Pre-cursor1, and Post-Cursor1 are in disabled state by default. However, Coefficient 2 (Main) is enabled when the Automatic main cursor is turned off.

### Output Timing
- Data Rate

Data Rate in Output Timing is always in disabled state.

### Error Insertion
- Insert Single Bit Error

In Error Insertion block, when Mode is selected as Error Ratio (Fixed spacing) or Error Ratio (Variable Spacing), on Turning ON error ratio insertion state, "Insert Single Bit Error" will be unavailable.

### Error Insertion
- Error Ratio

On selecting, Mode as Ctrl In A, Ctrl In B, Break, Sys In A, Sys In B Error Ratio will be disabled.

### Clock Out of Channels
- Output Timing
  - Frequency

Frequency is always in disabled state by default.

### Clock Out of M8045A Amplifier
- Termination Voltage

On selecting, Termination model as Balanced, Termination Voltage will be unavailable.

### Output Timing
- Frequency

Frequency is always in disabled state by default.

### Trigger Out Amplifier
- Termination Voltage

On selecting, Termination model as Balanced, Termination Voltage will be unavailable.

### Configuration
- Subrate Frequency

Whenever the Operating mode is Subrate clock, Subrate Frequency is in disabled state by default.

### Configuration
- Divider
- Subrate Frequency

On selecting operating mode as Sequencer Controlled, Divider and Subrate frequency will be unavailable.
### Functional block name | Parameters | Disabled parameters | Parameters that are non-configurable by default | Parameters that are non-configurable due to settings of other parameters
--- | --- | --- | --- | ---
Data In | Clock (Select Source as Clk In and Follow Sys clk is Enabled) | Symbol Rate, Clk In Frequency | Symbol Rate and Clk In Frequency are disabled. |  
| | Clock (Select Source as Clk In and Follow Sys clk is Disabled) | Clk In Frequency |  
| | Clock (Select Source as Sys Clk) | Follow Sys Clock, Clk In Multiplier, Clk In Frequency, Symbol Rate | Symbol Rate is in disabled state. | On selecting source as “Sys Clk”, Follow Sys Clk and Clk In Multiplier, Clk In Frequency will be unavailable.  
| Line Coding – PAM4 (Select PAM4-Uncoded OR Gray Coded) | Custom Symbol Mapping |  
| Comparator | Upper Threshold, Middle Threshold, Lower Threshold | Upper Threshold, Middle Threshold and Lower Threshold will be available under comparator block in case of PAM4 coding only. |  
| Input Timing | Data Rate | Data rate is always is disabled state. |  
| Alignment Results | All Parameters | All Alignment results will be in disabled state, irrespective of the line coding (NRZ or PAM4). |
Creating Groups in the Module View

The Module View allows you to create a group of available ports and simultaneously allows you to configure their parameters.

To create a group:

- Switch to Multiple Selection Mode by pressing Single Selection Mode icon.
- From your keyboard, hold the Ctrl key and select the ports from the modules. You need to select at least two ports in order to create a group.
- Right-click on the selected ports and click Create Group option or alternatively you can select the ports and click Create Group of Selection icon. A Create New Group dialog will appear as shown in the following figure:

![Create New Group](image)

- Provide a group name and press Create.

A new group will be created in the Group View.
System View

The **System View** displays the block diagram representation of the currently selected channel of the M8020A/M8030A. In addition, it also allows you to interactively modify the settings for each channel.

The **System View** user interface is shown in the following figure.

![System View Diagram](image)

The principal parts are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by the blue lines around block on mouse focus and the corresponding parameters are displayed in the **Parameters** window. The block may contain feature elements (for example, LF Jitter contain PJ and rSSC). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color.
Channels

Displays the channels that are connected to the module. You can select the channel on which you want to configure channel settings. You can assign a different color to each channel so that they are easily identified. For details, refer to Settings Window on page 535.

Using the Zoom Tool

The following figure shows the options provided by the zoom tool.

The zoom tools provide the following functionality:

- The Zoom In button allows you to enlarge the block diagram to view more details.
- The Zoom Out button allows you to reduce the block diagram.
- The Zoom Slider allows you to zoom in or zoom out the block diagram. The mouse wheel also provides a quick alternative to the zoom control. To zoom in and out using the mouse, hold down the [Ctrl] key while you turn the mouse wheel. Each click, up or down, increases or decreases the zoom factor by 25%.
- The Fit to View button fits the width of the block diagram so that the user does not have to scroll the block diagram to the right or to the left.
Understanding the System View

To understand the System View, let’s divide it into the following sections:

Generator

The following section of the System View represents the generator function:

It allows you to apply settings on the Data Out port or location (data generator).

It includes the following blocks:

- **State** - Click on the button to enable the outputs of Data Out for the selected channel. Once the outputs are enabled, the button changes to “ON”. If you press the button again, it will turn the state “OFF”.
- **Jitter** - Use this block to enable the jitter source of High Frequency Jitter, Low Frequency and Sweep. For more details on jitter, refer to Jitter Setup on page 284.
- **Intersymbol Interference** - Use this option to enable/disable ISI feature.
- **Shortcut for Impairment Setup View** - Use this shortcut to access the Impairment Setup View. For more details, refer to Impairment Setup View on page 172.
- **Interference** - Use this block to enable the interference (CMI or DMI). For details refer to Interference.
• Amplifier - This block represents the current value of Data Out's amplitude parameter. You can change the value by clicking on this block and modify the respective parameter in the Parameters window.
• Delay - Set the delay of the active edge of the data output.
• Data Generation - Acts as the output port for the generator which may be connected to the DUT.

Trigger

The following section of the System View represents the trigger function:

It allows you to apply settings on the Trigger Out port or location.

It includes the following blocks:
• State - Click on the button to enable the output of Trigger Output for the channel. Once the output is enabled, the button changes to “ON”. If you press the button again, it will turn the state “OFF”.
• Amplifier - Use this block to set the parameters related to amplifier of the trigger output.
• Output Timing - Use this block to set the delay of the active edge of the trigger output.
Clock

The following section of the System View represents the clock function:

The clock function allows you to apply settings on the Clock Out port or location. It includes the following blocks:

- **State** - Click on the button to enable the output of Clock Source. Once the output is enabled, the button changes to “ON”. If you press the button again, it will turn the state “OFF”.

- **Jitter** - Use this block to enable the elements of High Frequency Jitter, Low Frequency. For more details on jitter, refer to Jitter Setup on page 284.

- **Amplifier** - Use this block to set the parameters related to amplifier of the clock output.

- **Clock Divider** - Use this block to set a factor on which the output signal will be divided.

- **PLL Synthesizer** - This block represents the currently selected clock source. You can change the clock source by clicking on this block and the modify the respective parameter in Parameters pane. To enable the SSC state jitter source, click on the button. Once the SSC state is enabled, the button changes to “ON”. This is how the bit rate is set. For example, 5 GHz sets the bit rate to 5 Gb/s. If you press the button again, it will turn the state “OFF”.

![Clock Interface Diagram](image-url)
The following section of the System View represents the analyzer function:

Analyzer

The Analyzer function allows you to apply settings on the Data In port or location (analyzer). It includes the following blocks:

- **State** - Click on the button to enable the CDR state. Once the CDR state is enabled, the button changes to “ON”. For more details, refer to CDR Setup in M8020A/M8030A on page 342. If you press the button again, it will turn the state “OFF”.
- **Threshold** - Use this block to set the threshold of the input comparator.
- **Input Timing** - Use this block to set input timing delay.
- **Data Analysis** - Use this block to set input threshold and sampling point delay.
System View with M8061A Integration

This section describes the block diagrams provided by the System View when M8061A is integrated with other modules of M8020A.

Channels

Displays the channels that are connected to the M8020A. The following figure shows M1 (2 channels of M8041A), M2 (2 channels of M8051A) and M3 (M8061A) modules connected to the instrument.

![Channels Block Diagram](image)

When you select the channel, the corresponding block diagram of that channel appears which allows you to interactively configure channel settings. You can also assign a different color to each channel so that they are easily identified. For details, refer to Settings Window on page 535.

Integration Modes

The System View with M8061A integration provides the following modes:

- Standalone Mode
- Mux Only Mode
- Demux Only Mode
- Mux and Demux Mode

Standalone Mode

The Standalone mode is used to set the parameters of the Data Out port of M8041A module and Data In port of M8061A module.

The following figure shows the block diagram of M8041A module in Standalone mode:
The following figure shows the block diagram M8061A module in **Standalone** mode:
Mux Only Mode

The **Mux Only** mode is used to multiplex the signal in 2:1 ratio. In this mode, M8061A receives the non-inverted signal from the two Data Out ports of M8041A module and multiplex them in one channel in 2:1 ratio. Using this mode, you can set the parameters of Data Out port of M8061A module.

The following figure shows the connection diagram of **Mux Only** mode:

![Connection Diagram](image)

The following figure shows the block diagram M8041A module in **Mux Only** mode:

![Block Diagram](image)
Demux Only Mode

The Demux Only mode is used to de-multiplex the signal in 1:2 ratio. In this mode, the M8061A module provides the output to CDR module (N4877A) which de-multiplex the received signal in 1:2 ratio. Using this mode, you can set the parameters of Data Out and Data In ports of M8061A module.

The following figure shows the connection diagram of Demux Only mode:
The following figure shows the block diagram M8041A module in Demux Only mode:

![Block Diagram M8041A](image1)

The following figure shows the block diagram M8061A module in Demux Only mode:

![Block Diagram M8061A](image2)
Mux and Demux Mode

The **Mux and Demux** mode is used to multiplex the signal in 2:1 ratio and again de-multiplex the signal in 1:2 ratio. Using this mode, you can set the parameters of Data Out and Data In ports of M8061A module.

The M8061A expands the data rate up to 32 Gb/s and provides integrated and calibrated 4-tap de-emphasis (expandable to 8 taps).

The following figure shows the connection diagram of **Mux and Demux** mode:
The following figure shows the block diagram in **Mux and Demux** mode:
System View with M8062A Integration

This section describes the block diagrams provided by the System View when M8062A is integrated with other modules of M8020A.

M8062A Configuration

The following steps describe the procedure for M8062A configuration:

- Launch the M8070B software.
- If the Modules View is not already opened, go to Menu Bar > System and then click Module View.
- Locate the M8062A module. The following figure shows an example of Module View when an M8062A (M2) and an M8041A (M1) are installed in the M8020A system:

![Image of Module View](image.png)

The M8062A module cannot be used standalone. It must be used in combination with an M8041A module.

- Click the Configuration... button present on the M8062A module.
The **M8062A Configuration** dialog will appear as shown in the following figure:

- Make the connections as described in the above figure.
- Click **Enable**.
- For the block diagram representation and interactively modify the settings of the current mode, switch to **System View**. To do so, go to **Menu Bar > System** and then click **System View**.

**NOTE**
System view for M8062A is available only when 32G mode is enabled.
In 32G mode, access to some M8041A user controls are disabled to facilitate software control of this configuration.

The following figure shows the **System View** of the M8062A module:

In the M8062A **System View**, the principal parts are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by blue lines around the block on mouse focus. Parameters corresponding to the selected block are displayed in the **Parameters** window, on the right. The block may contain feature elements (for example, LF Jitter contains PJ and rSSC). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color. For more details, refer to **System View** on page 153.

In addition to the blocks that are described in the section **System View** on page 153, the M8062A **System View** has the following new blocks:
- **Clean Clk Out** - Half-rate, or divided, clock output with no applied jitter.
- **Clk In** - Pattern Generator clock input (half-rate). Connect to clock output of M8041A.
- **Clock Source** - Selects the clock source (CDR, System Clock or Clock In) for the M8062A DataIn port (Analyzer).
- **CDR** - Selecting “CDR” as the M8062A DataIn clock source enables the Analyzer CDR, so that incoming data is sampled using the recovered clock.
- **Auto Re-Lock** - When this feature is enabled (the default setting) the CDR will automatically re-lock when there is a loss of lock. When it is disabled, the CDR will only attempt to re-lock when manually initiated by clicking on the arrow next to the Auto Re-Lock On/Off button. It may be necessary to perform a manual re-lock after a pattern change.
- **High Transition Density** - For data patterns with high transition density, such as 1010 pattern, the CDR may have trouble gaining lock. Enabling the High Transition Density setting reduces the CDR’s internal gain to allow it to better lock on patterns with high transition densities. It may be necessary to perform a manual CDR re-lock after a change in the High Transition Density setting.
- **Optimize** - After the CDR has gained lock, certain condition changes, such as increasing applied jitter levels, can cause the analyzer to begin to measure errors. Executing the Optimize function causes the CDR to perform a finer alignment adjustment, which may result in a return to an error-free measurement.

**NOTE**
When using the Analyzer CDR, it may take a longer time to lock and achieve BER=0 after a frequency change than with the other clock sources.
M8040A System View

The **System View** displays the block diagram representation of the currently selected channel of the M8040A modules (M8045A and M8046A). In addition, it also allows you to interactively modify the settings for each channel.

The following figure shows the **System View** of channel 1 of the M8045A module (M1):
The following figure shows the **System View** of the M8046A module (M2):

The principal parts of the M8045A and M8046A **System View** are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by blue lines around the block on mouse focus. On clicking these blocks, the mostly used parameters are available which can be configured using the on-screen numeric keypad.

However, parameters corresponding to the selected block are displayed in the Parameters window, on the right. The block may contain feature elements (for example, HF Jitter contains PJ1, PJ2 and RJ). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color. For more details, refer to **System View** on page 153.
Impairment Setup View

The Impairment Setup View provides a tabular representation of the Impairment Sources and their corresponding parameters for each Data Out channel of the connected modules. This tabular visualization helps you to view, compare and configure the Impairment Source parameters for each channel in the same window.

How to Access the Impairment Setup View

The following are the two ways to access Impairment Setup View:

1. Through Menu Bar - Go to Menu Bar and then click System > Impairment Setup View. The Impairment Setup View will appear as shown in the following figure:

![Impairment Setup View](image)

2. Through System View - The Impairment Setup View can also be accessed through the System View by clicking on the Open Impairment View shortcut as shown in the following figure:

![Open Impairment View](image)
Features of the Impairment Setup View

In this tabular matrix of the Impairment Setup View, the rows consist of the Impairment Sources, their corresponding options and their related parameters. The columns represent channels Data Out, Clock and Trigger parameters for each channel.

Columns

Each channel of a module is represented using a particular color code, which form the column header and they correspond to the color-coding used for that channel in the Modules View. See Module View on page 123.

You may rearrange the column headers by clicking and dragging a header to the desired position.

For example, if you want to view the settings of M1Ch2 first, then click and hold the cursor on M1 Ch2, drag it to the right and release the cursor at the desired position.

The Impairment Setup View will now show the channel position as shown in the following figure:
Under each column's header, there are Low Frequency (LF) and High Frequency (HF) usage indicator. The Clock and Trigger has a Low Frequency indicator only. The following figure shows LF and HF indicator for channel 1 of module 1 (M1 Ch1):

These indicators display how much low frequency and/or high frequency is applied on each channel in percentage.

**Rows**

The Impairment Sources form the rows in the tabular matrix and have a hierarchical structure. To expand and view the options, click to the left of each Impairment Source.

The following list shows the Impairment Sources and their respective options that are available in the **Impairment Setup View**.

1. **Low Frequency (Jitter)**
   - PJ
   - rSSC

2. **High Frequency (Jitter)**
   - PJ1
   - PJ2
   - BUJ
   - RJ
   - sRJ
   - Sweep
3 Interference
   a ISI
   b CMI
   c DMI
4 Related Settings
   a SSC
   b Clk/2 Jitter

You can view, compare and even to configure the values of Impairments Source parameters for each channel. For more details on these Impairment Sources and their respective parameters, please refer to the chapter Setting up Generator on page 235.

Viewing Options in the Impairment Setup View

The Impairment Setup View provides the following viewing options:

- Collapse All
  This is the default viewing option of the tabular view.

Click on the Collapse All button to collapse the Impairment Sources rows, such that only the top-level hierarchy is displayed. In other words, in this view option, the options under each Impairment Source for the corresponding Data Out, Clock and Trigger of a channel are hidden.

- Expand Level 2 Groups
  This is one-level expansion of the tabular view.

Click on the Expand Level 2 Groups button to view options available under Impairment Sources. This view allows you to enable/disable the Impairment Sources options for corresponding channel.
• Expand All

This is two-level expansion of the tabular view.

Click on the button to view the parameters and the corresponding values for each option under the Impairment Sources. This view provides a full view of impairment setup view. Using this view, you can either enable or disable the Impairment Source options and also modify the parameter’s value for each channel.
How to set parameters in Impairment Setup View

To enable an option for an Impairment Source corresponding to a Channel or Clock and Trigger, select the check-box for the corresponding setting. To disable the option, unselect the check-box. The following shows an example how to enable the PJ option:

Some options available under the impairment sources are dependent on each other, such that enabling one or more option disables other options. Hover the mouse cursor on the tabular cells to understand the relational impact of such options, as shown in the example below.

The following are the dependencies which should be followed while configuring parameters:

- Sweep cannot be enabled if PJ is enabled.
- sRJ cannot be used if BUJ is enabled.
- RJ and BUJ cannot be used if sRJ is enabled.
- PJ and PJ2 cannot be used if Sweep is enabled.
• High Frequency Jitter profile of Clock and Trigger Out are controlled by Data Out of channel 1 as shown in the following figure:

![High Frequency Jitter profile](image)

The SSC can be enabled/disabled for all Data Out channels by a single option as shown in the following figure:

![SSC settings](image)

The option to either enable or disable SSC feature is available under Clock and Trigger column.

The Impairment Setup View also allows you to modify the parameter values. Depending upon whether the keypad option is enabled or disabled, the parameter values can be modified in the following ways:

• **When the keypad is enabled:** In this case when you click on the values which you want to modify, an on-screen numeric keypad appears as shown in the following figure:
Either type-in the values using the keyboard or use the on-screen numeric keypad to modify these values.
For more details on how to use the on-screen numeric keypad, refer to On-Screen Numeric Keypad on page 115.

- **When the keypad is disabled**: In this case, you are directly allowed to type-in the values using the keyboard.

**How to Use Filters**

Filters can be used to select the items to be displayed in the Impairment Setup View. In other word, it helps you to hide the items which are not required in the Impairment Setup View.

To apply filters, click on the 🎨 icon. This opens Items To Display window as shown in the following figure:
By default, all items (Channels and Parameters) in the **Items To Display** window are selected. However, you can select/unselect the check-box to show/hide the items. The changes are immediately reflected in the **Impairment Setup View**. For example, upon selecting M1 Ch1, M1 Ch2 under the Channels list and PJ under Jitter Types, the **Impairment Setup View** appears as shown below:
It is mandate to select at-least one channel. Failing this will display a message on the Impairment Setup View window that no channels are selected.

Notice that the icon appears on the top right of the Impairment Setup View which indicates that the filter has been applied.

If the channels are selected but their corresponding parameters are not selected, a message that no parameters are selected will be displayed.

The icon also appears in front of each item whose corresponding parameters are not selected. If you move the mouse pointer on this icon, a tool-tip message is displayed as shown in the following figure:
Group View

The Group View allows you to:
• Add/remove ports of a group.
• Set the properties of functional block of a group.

How to Launch Group View

The Group View is automatically launched when you create a group from the Module View. For details, refer to Creating Groups in the Module View on page 152. However, you also launch the Group View from the main GUI. To do so:
• Go to the Menu Bar > System and then select Group View.

The Group View will appear as shown in the following figure:

The Group View includes the following elements:
• Tool bar
• Group View
Tool bar

The tool bar includes the following elements to perform specific functions:

Table 47

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Create New Group</td>
<td>Opens the System Group Editor which allows you to create a new group. For more details, refer to Create New Groups in Group View on page 184.</td>
<td></td>
</tr>
<tr>
<td>Show Functional Block in Group</td>
<td>Use this toggle button to show functional blocks or locations in a group.</td>
<td></td>
</tr>
<tr>
<td>Show Edit Options</td>
<td>Use this toggle button to show/hide the group edit options.</td>
<td></td>
</tr>
<tr>
<td>Edit Existing Group</td>
<td>Opens the System Group Editor which allows you to edit the group. For details, refer to Edit Existing Group on page 186. This icon is only visible when the group is in the edit mode.</td>
<td></td>
</tr>
<tr>
<td>Delete Group</td>
<td>Deletes the group.</td>
<td></td>
</tr>
</tbody>
</table>

Group View

The Group View allows you to create, edit and delete a group. In addition, it also allows you to set the properties of functional block of the group. These features are further described in the upcoming sections of this chapter.
Create New Groups in Group View

To create a group in **Group View**:  
- Click **New Group** icon available on the tool bar. This will open the **System Group Editor**.  
- Select the ports or locations from the left side the **System Group Editor** and the preview of selected ports or locations will appear on right side. See the following figure:

![System Group Editor](image)

- Type a group name in the provided field and click **Create**. A new group will be created under that name.

Show Function Block/Location in Groups

The **Group View** allows you to set the group properties either through functional blocks or through locations in the group.

You can click ![icon](image) icon to switch to show functional blocks in the group. See the following figure:
The group is represented in the form of functional blocks available in the group. Once you click on the function block, the respective properties of the functional block are visible in the Parameters window. You can now set the properties of each functional block.

You can click icon to switch to show locations in the group. See the following figure:
The group is represented in the form of ports or locations available in the group. Once you click on the port or location, the respective properties of the port or location block are visible in the Parameters window.

The main advantage of the **Group View** is that it allows you to set the properties patterns/sequence of similar ports at once.

However, if you set the properties of the similar ports or locations that exists in different channels of a group, the properties of the ports or locations will not be applied. If you try to group the properties by clicking on the header of **Group View**, the corresponding value in the Parameters window will either be blank or show “?”.

See the following figure:

In this situation, you have to specify the property’s value which will be later applied to both ports or locations.

### Edit Existing Group

To edit an existing group;

- Click on the **Edit Existing Group** icon. This will open the **System Group Editor** window.
• Select the ports or locations from the left side of the **System Group Editor** and the preview of selected ports or locations will appear on right side. See the figure below:

![System Group Editor](image)

• Click **OK**. The group will be edited. However, if you provide a new group name in the provided field and click **OK**, a new group will be created under that name.

**Delete a Group**

You can also delete a group. To do so:

• Click on the **Delete Group** icon. It will open a **Delete Group** message box.

• Click **Delete**. The group will be removed from the view.
Setup View

The **Setup View** shows the block diagram of the pattern generator and error detector to provide a simple overview of the most important instrument settings at a glance.

**How to Access the Setup View**

The **Setup View** can be accessed on clicking the **Setup View** tab, once the M8070B software is launched. It can also be accessed through Menu Bar. Go to **Menu Bar** and then click **System > Setup View**. Please note that the **Setup View** user interface is different for each system, depending upon the connected modules. The following figure shows the **Setup View** for M8020A system (M8041A and M8051A):

Similarly, you can access the **Setup View** for M8020A/M8030A/M8040A system which can include M8041A, M8051A, M8061A, M8062A, M8045A, M8046A, M8195A, M8196A, clock recovery and real-time oscilloscope that can be controlled by M8070B.
Understanding Setup View

The Setup View interface includes a toolbar, a block diagram and a parameter window. All these GUI elements are described in the following section.

NOTE

The information about the GUI elements such as buttons and text fields, where the user inputs are required, are provided in the form of tooltip.

Toolbar

- **More Ports**
  The drop-down option allows you to configure the ports which are not available in the Generator or Analyzer blocks. On selecting a port, the respective parameters are displayed in the Parameters window.

- **Preset All**
  This option opens the “Preset Instrument State” dialog which resets the instrument state to factory default settings. For details, see section “Preset Instrument State” in the File Menu on page 90.
• **Zoom Tool**
  The following figure shows the options provided by the zoom tool.

![Zoom Tool Image](image)

The zoom tools provide the following functionality:
- The **Zoom In** button allows you to enlarge the block diagram to view more details.
- The **Zoom Out** button allows you to reduce the block diagram.
- The **Zoom Slider** allows you to zoom in or zoom out the block diagram.
- The mouse wheel also provides a quick alternative to the zoom control. To zoom in and out using the mouse, hold down the [Ctrl] key while you turn the mouse wheel. Each click, up or down, increases or decreases the zoom factor by 25%.
- The **Fit to View** button fits the width of the window so that the user does not have to scroll the block diagram to the right or to the left.

**Block Diagram**
This section shows the block diagram of the “Clock and Pattern Generator” pane and the “Analyzer-Detector” pane which is connected via a DUT Control. Each pane displays the functional blocks and their frequently used parameters. You can configure these basic parameters to perform a measurement.

The user interface provided by the block diagram provides the following features:
- **Channel Selection** - The channel selection for the Generator or Analyzer can be made using the drop-down list. Depending upon the selected channel, its corresponding block diagram will be displayed.

![Channel Selection](image)

Please ensure to enable the outputs by clicking on the **Global Outputs** button. The same can be done by clicking on the **Global Output** button present on the status bar.
• **Parameters Window** - Once, the channel section is made, you can configure the basic parameters of each functional block. However, you can also view and configure the detailed parameters on clicking the button, available at the top right of the block. All the parameters related to that functional block will be displayed in the **Parameter** window.

• **Clock and Pattern Generator pane**
  The “Clock and Pattern Generator” pane display the functional blocks which are related to clock generation and pattern generator. It may include Clock Generator, Clock Output, Trigger Output, Impairments, Pattern Data and Data Out 1 for a given channel. However, these functional blocks may vary, depending upon the type of module. In case of M8046A, the Data Out functional will show an additional **Coding** parameter. Similarly for other modules such as M8062A or AWG modules (M8195A/M8196A), the functional blocks may vary depending upon the channel selection.

• **Analyzer-Detector pane**
  The “Analyzer-Detector” pane display the functional blocks like DATA In which are related to error detection. It may include, Threshold, Equalization, CDR, depending upon the connected modules. For example, the CDR option will not be available for M8046A analyzer. This pane also provides access to various measurements which are supported by the selected analyzer channel. For example, the eye diagram and output level measurements will not be available for M8046A analyzer.
GUI Elements Description

The various GUI elements which are available in the block diagram are described below:

- **Check-Box** - You can use the check-box feature to enable/disable the feature such as Enable SSC, Enable CDR, etc. The following is an example of Enable SSC check-box:

  ![Enable SSC](image)

- **Toggle Button** - You can use the toggle button to enable the outputs such as clock output, trigger output, etc. The following is an example of Clock Output button:

  ![Clock Output](image)

- **Command Button** - You can also use the command buttons such as Break, Restart and Sync to perform some actions. The following is an example of Restart button:

  ![Restart](image)

- **Buttons that opens another window** - There are some buttons which takes you to another window such as Deemphasis..., CDR..., DUT Control.... When you click on these buttons, they open with the respective window/parameters. The following is an example of button which take you to Impairment View window:

  ![Impairment View](image)

- **Status Information** - Depending upon the analyzer's performance, this option provides the current status of the analyzer such as stopped CDR unlocked, sync loss, etc. The following is an example of analyzer status when there is a sync loss:

  ![Analyzer Status](image)
• **Measurement Selection** – Use this drop-down list to select the measurement. The measurement will be provided depending upon the selected analyzer channel.

![Measurement Views](image)

• **Status Indicator for Calculated BER/SER** – Indicates the status of the calculated BER/SER.

![BER 0.00e+00](image)

• **Measurement Preview** – Display the measurement preview of the currently run measurement. If you have already run the measurement once, it will show the status of last run measurement. You can double-click on the measurement preview to open the measurement window, provided the instance of that measurement is not closed. The following figure shows an example of measurement preview when the Jitter Tolerance measurement is executed.

![Measurement Preview](image)
How to perform a basic measurement

Follow the given steps to perform a basic measurement using a **Setup View**:

1. Open the **Setup View** window.
2. From the block diagram, select the channel for the “Clock and Pattern Generator” and “Analyzer-Detector” pane.
3. Use the available functional blocks to configure the required parameters for the “Clock and Pattern Generator” and “Analyzer-Detector” pane.
4. Click **Auto Align** button to start the BER threshold auto alignment. Click **Manual Alignment...** button, in case the manually aligning of the sampling point is required.
5. Select the measurement. It will take you to the respective measurement window.
6. Run the measurement. You will see the measurement preview on the “Analyzer-Detector” pane.
Controlling AWG(s) from M8070B User Interface

The M8070B system software allows to control AWGs (M8195A and M8196A) along with the M8020A/M8030A modules. Once the M8195A/M8196A AWG module is installed into an AXIe chassis, it can be accessed via the M8070B software. Ensure that you have latest version of M8070B software installed in your system. Also to access M8196A, you should have the latest version of M8070B and M8196A SFP (Rev 2.0.2.0 or above).

For complete details on M8195A Arbitrary Waveform Generator, visit www.keysight.com/find/m8195a.

For complete details on M8196A Arbitrary Waveform Generator, visit www.keysight.com/find/m8196a.

AWG(s) in Module View

Once the AWG integration is done, you will see a AWG module entry in the Module View. The following figure shows the Module View of M8195A/M8196A AWG:
Automatic Module Update in AWG(s)

The **Automatic Module Update** feature enables you to turn the automatic module updates ON or OFF. This feature is available on the right-side of the module or under the **System** parameters.

The following parameters are available for **System**:

- **Configuration**: The Configuration function has the following components:

  - **Automatic Module Update**: Enables or disables the automatic module updates. The same can be done by clicking the **Auto Update** button present on the Module View of AWG module.

  When the **Automatic Module Update** parameter is enabled, the modules state updates automatically, whenever a property is changed.

  When the **Automatic Module Update** parameter is disabled, the time intensive operation's execution defers for parameter changes. Depending on the module type, this may disable some or all the property updates. Additionally, it can also disable the dynamic parameter limit calculations, which can trigger the **Auto Correct Confirmation** dialog when the module updates.

- **Module Update Pending**: Applies the currently configured software state into module. This can also be done using the **Apply** button next to the Automatic Module Update ON/OFF toggle button. The same can be done by clicking the **Apply** button present on the Module View of AWG module. The orange **Apply** button indicates that the module update is pending.
M819xA Configuration

This section describes the steps to configure M8195A and M8196A AWGs.

M8195A Configuration

NOTE

M8195A Configuration option is not available for M8195A (Rev 1).

1. Click the Configuration... button. Depending upon the available channels in M8195A, the M8195A Configuration dialog will appear.
The following figure shows the **M8195A Configuration** dialog when four channels in M8195A are available:

2. Click on the radio button to select the memory mode. The following modes are available:

   - **One Channel Deep Memory**: The Data Out location of one channel will be sourced from extended memory and the other channels will be sourced from module internal memory. The data range in this mode is 256 Mb/s ... 65 Gb/s.
   
   - **Two Channels Deep Memory**: The Data Out locations of two channels will be sourced from extended memory and the other channels will be sourced from module internal memory. The data range in this mode is 256 Mb/s ... 32.5 Gb/s.
   
   - **Four Channels Deep Memory**: The Data Out locations of all four channels will be sourced from extended memory. The data range in this mode is 256 Mb/s ... 16.250 Gb/s.
   
   - **Random Interference**: The Data Out locations of all channels are used to Generate Random Interference.
   
   - **Sinusoidal Interference**: The Data Out locations of all channels are used to Sinusoidal Interference.

3. Click **Enable**.
M8196A Configuration

1. Click the Configuration... button. Depending upon the available channels in M8196A, the M8196A Configuration dialog will appear. The following figure shows the M8196A Configuration dialog when four channels in M8196A are available:

![M8196A Configuration Dialog](image)

2. Click on the radio button to select the memory mode. The following modes are available:
   - **Four Channels Deep Memory**: The Data Out locations of all four channels will be sourced from extended memory. The data range in this mode is 256 Mb/s ... 60 Gb/s.
   - **Random Interference**: The Data Out locations of all channels are used to Generate Random Interference.
   - **Sinusoidal Interference**: The Data Out locations of all channels are used to Sinusoidal Interference.

3. Click Enable.
Configuring AWG(s) Parameters

The M8195A/M8196A AWG has the **Data Out** and **Clk Gen** ports. You can use the **Parameters** window to configure these ports.

- **Line Coding** - Sets the line coding as NRZ or PAM4.
- **Amplifier** - The **Amplifier** function has the following components:
  - **Amplitude** - Sets the amplitude of the output signal.
  - **Offset** - Sets the offset voltage of output signal.
  - **High** - Sets the high voltage of output signal.
  - **Low** - Sets the low voltage of output signal.
- **Pulse Shaping Filter** - Sets the filter type used on the waveform. The filter type choices are Gaussian and Raised Cosine. Depending upon the specific waveform used, the waveform gets properties like transition time or roll-off factor. This parameter is only available in M8196A.
- **Roll-Off Factor** - Sets the roll-off factor for the raised cosine pulse shaping filter. This parameter is only available in M8196A.
- **Transition Time** - Sets the transition time (20%/80%) of data output signal.
- **Crossover** - Sets the data's crossover percentage.
- **Deemphasis** - Sets the deemphasis values in terms of coefficient values. You can set the two post-cursor, main cursor and two pre-cursor by adjusting the coefficient values. For details, see **De-Emphasis Signal Generator** on page 252.
- **Output Timing** - Sets the delay of the output data signal.
- **HF Jitter** - Enables and sets the high frequency jitter.
- **Embedding** - Sets the S-Parameter for embedding.
- **De-Embedding** - The **De-Embedding** function has the following components:
  - **Channel Specific** - Applies channel specific correction of the amplitude and phase using an internal calibration.
  - **Standard Cable** - Defines whether the signal should be pre-distorted considering the properties of the standard cable set.
  - **S-Parameter State** - Enables/Disables S-Parameter compensation.
  - **S-Parameter Profile** - Selects the S-Parameter profile. It also allows you to import and export a S-Parameter profile.
  - **S-Parameter Output Port** - Selects the output port in S-Parameter profile.
• **S-Parameter Input Port** - Selects the input port in S-Parameter profile.

• **Clk Gen** - The Clk Gen port has the following components:
  - **Synthesizer** - Used to set data rate frequency and period.

• **Random Interference** - The Random Interference function has the following components:
  - **Crest Factor Unit** - Used to set the random interference crest factor unit type. Following unit types are allowed:
    - **Linear** - This is the default setting. Select this unit to specify the crest factor as voltage ratio.
    - **Logarithmic** - Select this unit to specify the crest factor in dB.
  - **Crest Factor** - Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
  - **Highest Frequency** - Used to set the random interference high frequency in Hz.
  - **Lowest Frequency** - Used to set the random interference low frequency in Hz.

• **Sinusoidal Interference** - The Sinusoidal Interference function has the following components:
  - **Frequency** - Used to set the sinusoidal interference frequency in Hz.

For M8195A, the frequency may be set up to 32 GHz and for M8196A, the frequency can be set up to 46 Gb/s. This is applicable for both NRZ and PAM4 line coding.
Simultaneous Injection of CMSI and DMSI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate common mode sinusoidal interference (CMSI) and differential mode sinusoidal interference (DMSI) on an output signal. CMSI/DMSI is an extension of existing sinusoidal interference.

Follow the given steps to generate multi-tone CMSI/DMSI on the output signals:

1. In the M819xA Configuration dialog, select Sinusoidal Interference and then click Enable.

For more information on Configuration dialog, see M819xA Configuration on page 197.

2. Set the parameters to generate multi-tone CMSI/DMSI. For details on parameters, see M819xA AWG CMSI and DMSI Parameters on page 203.
M819xA AWG CMSI and DMSI Parameters

The following functional blocks are available in the Parameter Window to generate CMSI and DMSI.

- **Channel Configuration**
  - **Channel Coupling** – The channel coupling provides the flexibility to couple the two channels. Depending upon the availability of channels in a module, the channels can be coupled in the following ways:
    - **Four channel Module**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/4

Use the drop-down option to select the channels. For example, selecting “1/2” will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

Physical connection changes are required for the channels to be coupled. If two channels (Channel 1 and Channel 2) are coupled, then the differential pair cable must be connected to the non-inverted ports of channel 1 and channel 2. Ensure to terminate the unused output ports with 50 Ohms.

The following block diagram provides an example how to cable the normal/complement outputs of AWG to couple channels 1 and 2:

Select “None”, if you don’t want to use the multi-tone functionality.

- **Amplifier** – This functional block has the following parameters:
  - **Output State** – Turns on/off the state of the output.
- **Termination Voltage** – Sets the external termination voltage.
- **Amplitude** – Sets the amplitude of the output signal. Once, the channels are coupled, this parameter will be in disabled state. However, the value of this parameter depends on the value of **Amplitude 1**.
- **Offset** – Sets the offset of the output signal.
- **Amplitude Correction Factor** – Sets the amplitude correction factor. The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channels.

The **Amplitude Correction Factor** parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.

- **Sinusoidal Interference** – This functional block allows you to set Tone Mode, Frequency, Amplitude and Phase for individual signal (1/2). It has the following parameters:
  - **Tone Mode (1/2)**: Sets the tone mode of the output signal. The available options are:
    - **Off** – In this case, the selected tone mode is will not participate.
    - **Common Mode** – In this case, Common Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
    - **Differential Mode** – In this case, Differential Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
  - **Amplitude (1/2)**: Sets the amplitude of selected tone (1/2). Please note that the value of Amplitude 1 will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across both tones must be between 0 to 995 mV.
  - **Frequency (1/2)**: Sets the frequency of the selected tone (1/2).
  - **Phase (1/2)**: Sets the phase of the selected tone (1/2).
Simultaneous Injection of CMRI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate common mode random interference (CMRI) on an output signal. CMRI is an extension of existing random interference.

Follow the given steps to generate CMRI on the output signals:
1. On the right-side of the module, click Configuration.

2. In the M819xA Configuration dialog box, select Random Interference, and then click Enable.

3. Set the parameters to generate CMRI. For details on parameters, see M819xA AWG CMRI Parameters on page 206.
M819xA AWG CMRI Parameters

The following functional blocks are available in the Parameter Window to generate CMRI.

- **Channel Configuration**
  - **Channel Coupling** – The channel coupling provides the flexibility to couple the two channels. Depending upon the availability of channels in a module, the channels can be coupled in the following ways:
    - **Four channel Module**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/4

  Use the drop-down option to select the channels. For example, selecting “1/2” will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

Select “None”, if you don’t want to generate CMRI.

Physical connection changes are required for the channels to be coupled. Ensure to terminate the unused output ports with 50 Ohms.

- **Amplifier** – This functional block has the following parameters:
  - **Output State** – Enables or disables the state of the output.
  - **Termination Voltage** – Sets the termination voltage of the output signal.
  - **Amplitude** – Sets the amplitude of the output signal.
  - **Offset** – Sets the offset voltage of the output signal.
  - **Amplitude Correction Factor** – Sets the amplitude correction factor. The Amplitude Correction Factor parameter is not included in the coupling and so it can be set independently on each coupled channel.

  The Amplitude Correction Factor parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

  The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.
- **Random Interference** - The Random Interference function has the following components:
  - **Crest Factor Unit** - Used to set the random interference crest factor unit type. Following unit types are allowed:
    - **Linear** - This is the default setting. Select this unit to specify the crest factor as voltage ratio.
    - **Logarithmic** - Select this unit to specify the crest factor in dB.
  - **Crest Factor** - Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
  - **Highest Frequency** - Used to set the random interference high frequency in Hz.
  - **Lowest Frequency** - Used to set the random interference low frequency in Hz.
AWG as External Level Interference (RI/SI) Source

The Keysight M8195A and M8196A AWG can be used as external level interference source with sinusoidal and random modulation. For this you need to select ‘Random Interference’ or ‘Sinusoidal Interference’ from the M8195A and M8196A configuration dialog. For more details on the M8195A and M8196A configuration dialog, refer to M8195A Configuration on page 197 and M8196A Configuration on page 199. The M8070B system software allows controlling interference parameters such as amplitude, highest frequency, lowest frequency and crest factor. Keysight provides a matched directional coupler pair (orderable option M8045-802) for injecting the RI or SI signal before or after the channel. Specifications for external level interference sources RI/SI with M8195A, M8196A can be found in M8040A data sheet.

The following block diagram shows the recommended RX test setup with RI/SI source (M8195A/M8196A):
System View with AWG(s) Integration

This section describes the block diagram provided by the System View when AWG module is integrated in M8070B. The System View for AWG varies on the number of channels available on M8195A or M8196A.

The following figure shows System View of M8195A/M8196A when all four channels are available.

The System View of AWG shows four Data Out channels in the same window. The principal parts of the System View are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by blue lines around the block on mouse focus. On clicking these blocks, the mostly used parameters are available which can be configured using the on-screen numeric keypad. However, parameters corresponding to the selected block are displayed in the Parameters window, on the right. The block may contain feature
elements (for example, HF Jitter contains PJ1, PJ2 and RJ). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color. For more details, refer to System View on page 153.

Signal Generation in AWG

For detailed information about signal generation on arbitrary waveform generators of the M81XX class can be found in the document named "Fundamentals of Arbitrary Waveform Generation" which can be downloaded from here: www.keysight.com/find/awg-apps
Using AWG Frequency Response Calibration for Improved Signal Performance

Keysight recommends performing signal calibration within the AWG system (M8195A/M8196A) for DUT testing.

In other words, the specific channel of the AWG must be calibrated with specific cables and connectors that are used between the AWGs DATA OUT and the DUTs RX port.

To perform the phase/frequency response calibration, you require a DCA-X and DCA-M sampling scope with a receiver module above 30 GHz. Alternatively, you may use a DSA-Z series real-time scope, which is capable of signal analysis above 30 GHz. Generally, a better signal quality is achieved when this calibration is performed using a sampling scope as compared to the calibration performed using a real-time scope.

A S-Parameter file is generated as a result of performing this calibration using IQTools, which can be imported as a De-Embedding filter into the M8070B software. For details on how to perform these steps, refer to IQToolsPhaseFrequencyResponseCalibration.pdf, which is available within the M8070B documentation folder.

Selecting Line Coding

You can define the line coding for a M8195A/M8196A Data Out port through the Parameters window. The M8195A/M8196A Data Out port supports NRZ and PAM4 line coding.

![Line Coding](image)

Make sure to use the similar line coding of all Data Out ports assigned to the same sequence of M8195A/M8196A. An "Auto Correction" window will appear if you select different line coding. Clicking on the "Allow" button present on this window, applies the same line coding on all Data Out ports.
The PAM4 line coding provides the symbol mapping options as shown in the following figure:

- **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 01 maps to symbol 1, 10 maps to symbol 2 and 11 maps to symbol 3.
- **Gray Coded** - In this mapping, the bit sequence 00 maps to symbol 0, 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.
- **Custom** - In this mapping the consecutive data bits are mapped to symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10). The position within this list corresponds to the symbol level. First value is for Symbol 0 and the last value is for Symbol 3.
- **Symbol Level** - It controls the PAM4 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM4 symbol. The levels of PAM4 symbol 0 and 3 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.
Creating Patterns for AWG(s)

The M8070B software provides **Pattern Editor** for M8195A/M8196A module as well. The functionality of the **Pattern Editor** is same as for other modules. You can create, edit, load patterns and perform the pattern settings in the same way as done for other modules. For more details, refer to **Pattern Editor** on page 425.

However for bit coded patterns, the **Pattern Editor** allows you to view the symbols in the **PAM4 No Coding** and **PAM4 Gray Coding**. These options are available in the **Settings > Data View Mode**.

The following figure shows an example of bit symbol, viewed in the **PAM4 Gray Coding**.

![Example of bit symbol, viewd in PAM4 Gray Coding](image)

In the **PAM4 No Coding** mode, the bit sequence 00 maps to symbol 0, 10 maps to symbol 2 and 11 maps to symbol 3.

In the **PAM4 Gray Coding** mode, the bit sequence 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.

Sequence Settings for AWG(s)

The M8070B software provides **Sequence Editor** which can be used with most of the devices supported by M8070B. The functionality of the **Sequence Editor** is the same as for other modules. You can create, edit, load patterns and perform sequence settings in the same way as done in
the M8070B sequence editor. You can change pattern type as static, clock, PRBS, memory pattern, in single block with infinite loop. For more details, refer to Sequence Editor on page 389.

The M819xA modules can also be configured from the M8070B Sequence Editor. The following figure shows the AWG(s) Sequence Editor:

You can use the Sequence Settings window to reprogram the values of AWG parameters.

Parameters which are not applicable for AWG modules will be either hidden, disabled, or checked when performing a sequence download.

The Sequence Editor when used with an AWG module, has the following capabilities:

- A single block can be looped infinitely
- Supports the following block types:
  - PRBS (all polynomials that fit into AWG memory)
  - Memory
  - Static 0 or 1
  - Single pulse per block
  - Clock
Jitter Setting in AWG(s)

The AWG integration into the M8070B software supports sinusoidal jitter, random jitter and spread spectrum clocking (SSC).

Sinusoidal jitter and random jitter can be turned on and off per channel while SSC can only be activated per module.

Periodic Jitter (Valid for PJ1, PJ2 and SSC)

When defining a sequence referencing a specific pattern it will automatically be generated containing the specified jitter. For example in case the given pattern has a duration of 1 µs for the selected baud rate and the jitter period is 2 µs it would not be possible for this jitter to correctly appear inside the pattern. To handle this a second iteration of the pattern is appended giving the memory segment a total duration of 2 µs. With this it is possible for the resulting waveform to contain the selected jitter.

A side effect of this procedure is that the required sample memory for a selected pattern changes depending on the selected jitter components.

In case the jitter cannot be mapped to the available memory while adhering to the jitter accuracy defined in the data sheet a warning message will be displayed to make the user aware of this shortcoming.

Measuring Periodic Jitter

When measuring periodic jitter on an oscilloscope it is important to note that the jitter period will always be rounded in a way that the effective pattern length (which may contain multiple iterations of the user defined pattern) is a multiple of this jitter period.

Another thing to note is that for short pattern, high jitter frequency and the case where the data rate is an integer multiple of the jitter frequency the effective pattern can become maximally short. This will be observable by a relatively fast start of waveform playback but can have an impact on the measured jitter histogram.

For the above mentioned cases the number of distinct edge deviations from their non-jittered positions can be limited which leads to a histogram containing only a low number of lines.

To tweak the quality of the jitter histogram it is possible to use a larger pattern e.g. by repeating the shorter pattern multiple times in the pattern file or using an odd number for the jitter frequency.
Random Jitter (RJ)

The given pattern will be generated with the selected random jitter parameters. Definable are thereby a low pass and high pass frequency which limits the contained jitter components.

Measuring Random Jitter

As the waveform is completely pre-calculated it is not possible to generate truly random jitter with this approach.

Similar to the periodic jitter case it is also true for random jitter that short patterns will not lead to a realistic looking jitter histogram. If a better jitter quality is desired it is therefore necessary to use a longer pattern. In case the actual pattern needs to be short it is possible to have it repeat multiple times in the pattern file and thereby obtain different edge deviations on a single symbol.
Controlling M8054A from M8070B System Software

The M8070B system software allows you to control the M8054A interference source module along with the M8020A/M8030A/M8040A modules. Once the M8054A interference source module is installed into an AXIe chassis, it can be accessed via the M8070B software.

Ensure that you have the latest version of M8070B (version 6.5 or later) and M8054A software installed in your system.

You can control the following interference parameters for the M8054A interference source through M8070B system software.

- Random Interference
  - Channel Coupling
  - Amplifier
  - Random Interference
- Sinusoidal Interference
  - Channel Coupling
  - Amplifier
  - Sinusoidal Interference
M8054A in Module View

The following figure shows the **Module View** of M8054A.
M8054A Configuration

Follow the steps to configure the M8054A interference source.

1. On the right-side of the module, click Configuration.

2. On the M8054A Configuration dialog box, select one of the following:
   - **Random Interference**: The DataOut locations of all channels are used to generate random interference.
   - **Sinusoidal Interference**: The DataOut locations of all channels are used to generate sinusoidal interference.

3. Click Enable.

M8054A Parameters configuration

The M8054A interference source has the Data Out and System ports. You can use the Parameters window to configure these ports.

The following parameters are available for Data Out:

- **Channel Configuration**: The Channel Configuration function has the following components:
  - **Channel Coupling**: Provides the flexibility to couple two channels. Depending upon the availability of the channels in a module, the channels can be coupled in the following ways:
    - **Four channel Mode**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/2

Use the drop-down option to select the channels. For example, selecting "1/2" will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.
Select “None”, if you don’t want to use the multi-tone functionality.

Physical connection changes are required for the channels to be coupled. If two channels (Channel 1 and Channel 2) are coupled, then the differential pair cable must be connected to the non-inverted ports of channel 1 and channel 2. Ensure to terminate the unused output ports with 50 Ohms.

Using this configuration, you can use common mode sinusoidal interference (CMSI)/differential mode sinusoidal interference (DMSI).

- **Amplifier**: The Amplifier function has the following components:
  - **Output State**: Enables or disables the state of the output.
  - **Termination Voltage**: Sets the termination voltage of the output signal.
  - **Amplitude**: Sets the amplitude of the output signal.
  - **Offset**: Sets the offset voltage of the output signal.
  - **Amplitude Correction Factor**: Sets the amplitude correction factor. The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channels.

  The **Amplitude Correction Factor** parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

  The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.

  - **Sinusoidal Interference**: The Sinusoidal Interference function has the following components:
    - **Frequency**: Sets the frequency of the output signal.

  - **Random Interference**: The Random Interface function has the following components:
    - **Crest Factor unit**: Used to set the random interference crest factor unit type. Following unit types are allowed:
      - **Linear**: This is the default setting. Select this unit to specify the crest factor as voltage ratio.
      - **Logarithmic**: Select this unit to specify the crest factor in dB.
• **Crest Factor**: Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.

• **Highest Frequency**: Used to set the random interference high frequency in Hz.

• **Lowest Frequency**: Used to set the random interference low frequency in Hz.

The following parameters are available for **System**:

• **Configuration**: The Configuration function has the following components:

  ![Configuration](image)

  **Automatic Module Update**: Enables or disables the automatic module updates. The same can be done by clicking the **Auto Update** button present on the Module View of AWG module.

  ![Auto Update](image)

  When the **Automatic Module Update** parameter is enabled, the modules state updates automatically, whenever a property is changed.

  When the **Automatic Module Update** parameter is disabled, the time intensive operation's execution defers for parameter changes. Depending on the module type, this may disable some or all the property updates. Additionally, it can also disable the dynamic parameter limit calculations, which can trigger the **Auto Correct Confirmation** dialog when the module updates.
- **Module Update Pending**: Applies the currently configured software state into module. This can also be done using the **Apply** button next to the Automatic Module Update ON/OFF toggle button. The same can be done by clicking the **Apply** button present on the Module View of AWG module. The orange **Apply** button indicates that the module update is pending.

**NOTE**

This parameter cannot be changed directly. When the Automatic Module Update parameter is enabled, the Module Update Pending parameter changes to OFF automatically.

**NOTE**

The module update pending indication will not detect the changes done to (externally) referenced files or when bypassing the user interface. An example of this effect is a pattern file which is edited while being referenced by a sequence bound to the concerned module. Another example is a selected S-Parameter file which is modified directly on the file system.

To update the module in these cases, it is necessary to perform a full module update by triggering the module update command.
Simultaneous Injection of CMSI and DMSI Using M8054A

The channels of M8054A can be coupled to generate common mode sinusoidal interference (CMSI) and differential mode sinusoidal interference (DMSI) on an output signal. CMSI/DMSI is an extension of existing sinusoidal interference.

Follow the given steps to generate multi-tone CMSI/DMSI on the output signals:

1. On the right-side of the module, click Configuration.

2. On the M8054A Configuration dialog box, select Sinusoidal Interference, and then click Enable.

3. Set the parameters to generate multi-tone CMSI/DMSI. For details on parameters, see M8054A CMSI and DMSI Parameters.
M8054A CMSI and DMSI Parameters

The following functional blocks are available in the Parameters Window to generate multi-tone CMSI/DMSI.

- **Channel Configuration**: The Channel Configuration function has the following components:
  - **Channel Coupling**: Provides the flexibility to couple two channels. Depending upon the availability of the channels in a module, the channels can be coupled in the following ways:
    - **Four Channel Module**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/2
  
  Use the drop-down option to select the channels. For example, selecting "1/2" will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

  Select "None", if you don't want to use the multi-tone functionality.

  When the channel coupling is enabled, the parameters of both the coupled channels are synced automatically. Physical connection changes are required for the channels to be coupled. If two channels (Channel 1 and Channel 2) are coupled, then the differential pair cable must be connected to the non-inverted ports of channel 1 and channel 2. Ensure to terminate the unused output ports with 50 Ohms.

- **Amplifier**: The Amplifier function has the following components:
  - **Output State**: Enables or disables the state of the output.
  - **Termination Voltage**: Sets the termination voltage of the output signal.
  - **Amplitude**: Sets the amplitude of the output signal.
  - **Offset**: Sets the offset voltage of the output signal.
  - **Amplitude Correction**: Sets the amplitude correction factor.

  The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channel.

  The **Amplitude Correction Factor** parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.
The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.

- **Sinusoidal Interference**: This functional block allows you to set Tone Mode, Frequency, Amplitude and Phase for individual signal (1/2). It has the following parameters:
  - **Tone Mode (1/2)**: Sets the tone mode of the output signal. The available options are:
    - **Off**: In this case, the selected tone mode will not participate.
    - **Common Mode**: In this case, Common Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
    - **Differential Mode**: In this case, Differential Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
  - **Frequency (1/2)**: Sets the frequency of the selected tone (1/2).
  - **Amplitude (1/2)**: Sets the amplitude of selected tone (1/2). Please note that the value of Amplitude 1 will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across both tones must be between 0 to 995 mV.
  - **Phase (1/2)**: Sets the phase of the selected tone (1/2).
Simultaneous Injection of CMRI using M8054A

The channels of M8054A can be coupled to generate common mode random interference (CMRI) on an output signal. CMRI is an extension of existing random interference.

Follow the given steps to generate CMRI on the output signals:
1. On the right-side of the module, click Configuration.

2. On the M8054A Configuration dialog box, select Random Interference, and then click Enable.

Set the parameters to generate CMRI. For details on parameters, see M8054A CMRI Parameters.
M8054A CMRI Parameters

The following functional blocks are available in the Parameters Window to generate multi-tone CMRI.

- **Channel Configuration**: The Channel Configuration function has the following components:
  - **Channel Coupling**: Provides the flexibility to couple two channels. Depending upon the availability of the channels in a module, the channels can be coupled in the following ways:
    - **Four channel Mode**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/2
  
  Use the drop-down option to select the channels. For example, selecting "1/2" will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

  Select "None", if you don't want generate CMRI.

  Physical connection changes are required for the channels to be coupled. Ensure to terminate the unused output ports with 50 Ohms.

- **Amplifier**: The Amplifier function has the following components:
  - **Output State**: Enables or disables the state of the output.
  - **Termination Voltage**: Sets the termination voltage of the output signal.
  - **Amplitude**: Sets the amplitude of the output signal.
  - **Offset**: Sets the offset voltage of the output signal.
  - **Amplitude Correction Factor** – Sets the amplitude correction factor. The Amplitude Correction Factor parameter is not included in the coupling and so it can be set independently on each coupled channels.

  The Amplitude Correction Factor parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

  The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.
Random interference: The Random interference function has the following components:

- **Crest Factor unit:** Used to set the random interference crest factor unit type. Following unit types are allowed:
  - **Linear:** This is the default setting. Select this unit to specify the crest factor as voltage ratio.
  - **Logarithmic:** Select this unit to specify the crest factor in dB.
- **Crest Factor:** Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
- **Highest Frequency:** Used to set the random interference high frequency in Hz.
- **Lowest Frequency:** Used to set the random interference low frequency in Hz.

M8054A as External Level Interference (RI/SI) Source

The M8054A is an external level interference source with Random and Sinusoidal modulation. For this, you need to select ‘Random Interference’ or ‘Sinusoidal Interference’ from the M8054A configuration dialog box. For more details on the M8054A configuration, refer to M8054A Configuration. The M8070B system software allows controlling interference parameters such as amplitude, highest frequency, lowest frequency, crest factor and so on.

Keysight provides a matched directional coupler pair (M8045A-802) and a matched coupler pair (M8045A-803) for injecting the RI or SI signal before or after the channel. Specifications for external level interference sources RI/SI with M8054A can be found in M8040A data sheet.
System View of M8054A

This section describes the block diagram provided by the System View when M8054A module is integrated in M8070B. The System View for M8054A varies on the number of channels available.

The principal parts of the System View are represented by blocks, and these blocks are connected by lines/arrows. When a block is selected, the corresponding parameter values are displayed under the Parameters pane. The selected block is highlighted by blue borders. For more details, refer to System View.
Extended Sequencing Capabilities in AWGs

Basic Sequencing

This section describes how patterns are generated in case only a single infinitely looped sequence block is defined. This basic sequencing description is valid for M8195A and M8196A modules.

- PRBS, Static, and Clock sequence block types are repeated with their minimum possible granularity ignoring the number of symbols specified in the sequence block length.
- Memory Patterns and Pulses are created with the chosen pattern length using the sequence block length as the minimum repetition rate.

Extended Sequencing

Pattern Generation

This section describes how the distinct sequence block types are generated when using the enhanced AWG sequencing capabilities in M8070B. Presently, these capabilities are only available with M8195A modules which are configured with the 'SEQ' option meant for sequencing.
• **PRBS**

In a looping sequence block, a PRBS pattern is generated using the specified sequence block length as a minimum number of bits and increased to a full repetition of the base PRBS. As an example, a PRBS7-1 with original length of 127 bits and a sequence block length of 200 bits is given. This will generate a PRBS pattern with a length of 254 bits, meaning two PRBS7-1 iterations. These 254 bits are then used as a base pattern for the generated waveform and multiplied as required to fit into an AWG memory segment.

Non-looping patterns contain the number of sequence bits defined in the sequence block and do not consider the natural PRBS repetition length.

• **Memory Pattern**

For memory patterns, only the number of bits that are specified as sequence block length, occur in the resulting pattern. In case the memory pattern has a length of 200 bits while the sequence block length is specified as 100 bits, only the first 100 bit of the memory pattern will be used for generating the data stream.

• **Static**

Static segments use the number of bits in the sequence block, either as a minimum repetition length for roll-out in looped sequence blocks or for defining a minimum pattern length in non-looped sequence blocks.

• **Clock**

The minimum number of clock symbols are defined by the least common multiple of the clock divider setting and the number of bits specified as sequence block length. In case the line coding is, for example defined as PAM4, the number of bits of a clock sequence block additionally needs to be divisible by the number of bits per symbol which is 2 bit/symbol.

• **Pulse**

The pulse pattern considers the number of bits specified as sequence block length as the minimum pattern length. The length of the pulse’s high duration is thereby specified by the width property configurable in the sequence block’s data properties. In case of a line coding containing more than one bit per symbol, the pulse pattern width and length must be a multiple of the bits per symbol value (For PAM4, this value is 2 bit/symbol).
Block Settings

Sequence Block

A sequence block can contain an arbitrary user defined pattern, but the effective length of such a sequence block is enlarged internally to fit all the granularity requirements. This leads an effectively sent waveform to be separated into two distinct parts. One part is dubbed as payload (containing the desired pattern) while the other part is called extension (required to meet hardware limitations).

It is ensured that the sequence block length always contains an integral number of symbols. Additionally, the number of sequence block symbols is divisible by two, which allows to stay in sync with a half rate clock signal across multiple sequence blocks.

Sequence Block

<table>
<thead>
<tr>
<th>Payload</th>
<th>Extension</th>
</tr>
</thead>
</table>

Traditionally, a sequence block contains only the desired pattern but for M8195A modules, a non-looped sequence block contains a payload and extension pattern part.

- **Payload**
  - It consists of the user-defined pattern. The data sent during the payload duration is provided from a memory pattern location, PRBS selection, etc.
  - The location of the payload inside a sequence block is selectable. Following are the available choices for pattern alignment:
    - Align payload to sequence block start
    - Align payload to sequence block end

- **Extension**
  - The extension part is necessary because of limitations such as sequencer linkage across multiple channels, AWG sample memory granularities, module-wide sample rate and so forth. It extends the waveform sent during playback of a non-looped sequence block to match all preconditions.
The data content of the extension pattern is selectable. Following are the selectable block fill modes:

- **Use Adjacent Symbol Value**
  
  Depending on payload alignment, this setting uses the first or the last symbol value of the payload pattern for filling up the sequence block.

  Using this option will generally produce the shortest sequence block duration with the smallest extension pattern.

- **Repeat Pattern**
  
  This setting repeats the payload inside the extension block. Using this setting, the entire sequence block containing an integral number of payload repeats. This setting produces the same output, independent of the selected payload alignment mode.

  This option generally causes the extension pattern length to increase as it needs to allow for accommodating multiples of the payload pattern length.

- **Fill Extension with Clock Signal**
  
  This option fills the extension pattern with a half rate clock.
Event Configuration

The M8070B software system supports some of the hardware triggering capabilities of M8195A. These features can be configured via the modules view when accessing the 'Trig In', 'Event In', or 'Event Config' functional blocks.

Trig In and Event In

These blocks allow configuration of the input comparator state of the AWG module by defining a decision threshold voltage and an input detection polarity. An event is asserted from the respective input in case the detected voltage transitions above the defined threshold voltage for positive polarity or below the threshold voltage for negative polarity.

Event Config

In this functional block, it is possible to configure whether "Trig In" or "Event In" is connected to trigger a conditional break event in a multi-block sequence. Using M8195A SFP (Soft Front Panel), the advance event corresponds to the conditional break event in M8070B.

By using the break command from the sequence editor it is possible to fire the "Force (Advance) Event" in the SFP. Additionally, it is possible to enable or disable the hardware advance event by using the "Advance Event State" switch.

SCPI Commands

The advance sequencing can also be executed using the remote programming. For details of these commands, refer to M8000 Series Programming Guide.
5 Setting up Generator

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Overview

The M8020A/M8030A/M8040A generator generates an output signal based on a data pattern. It has the following possibilities for generating an output signal:

• Providing a wide range of clock frequencies
  You can use the generator's internal clock or an external clock for defining the frequency of the outgoing stream.

• Distorting the signal by adding jitter
  You can connect an external delay control device (for example a function generator) to add jitter to the generated signal.

• Adding errors to the output stream
  The M8020A/M8030A/M8040A can be set up to insert errors into the outgoing stream either internally, according to an external signal, or manually (from the operator).

• Run-time switching between two patterns
  You can set up two patterns and switch between them during runtime either automatically, according to an external signal, or manually.

• Suppressing the output stream
  The output signal can be suppressed according to an external signal.

The M8020A/M8030A/M8040A generator also provides output ports that let you connect an external instrument, such as an oscilloscope.
M8020A/M8030A Generator Ports

The M8020A/M8030A generator ports are used to set the generator’s clock frequency and to define the output signal with respect to jitter, error insertion and signal output. In addition, the generator’s output ports are also used to supply a clock signal and trigger (for example, analyzer), and an arbitrary data signal for testing your device.

The M8020A/M8030A provides a high level of integration with built-in clock synthesizer, de-emphasis, jitter and level interference. It allows you to set the parameters for the built-in generator parameters such as amplifier, de-emphasis, HF and LF jitter, common mode interference and differential mode interference.

The following figure shows the M8020A/M8030A generator’s ports.

The M8020A/M8030A generator’s ports include the following:

- **Ref Clock In**
  The Ref Clk In input can be used as reference frequency or as external system frequency directly for the instrument. An external provided signal can be measured at that input. This input is tightly involved in the system frequency generation.

- **Data Out and Data Out**
  The differential data output serve as device stimuli and can be set up so that they are compatible with a variety of logic families. With respect to Data Out, Data Out has inverted logic.

- **Clock Out and Clock Out**
  The differential clock output serve as frequency (bit rate) reference and can be set up so that they are compatible with a variety of logic families. With respect to Clock Out, Clock Out has inverted logic.
• Trigger Out and Trigger Out
  This port allows you to trigger another device (for example, an oscilloscope) and can be set up so that they are compatible with a variety of logic families. Trigger Out has more modes, e.g. sub rate clock to be used as ref clock for a DUT. With respect to Trigger Out, Trigger Out has inverted logic.

• Sys Out A/B
  The system level control outputs used to trigger events to the DUT or external instruments.

• Ctrl Out A
  The control output port provides the Error Output functionality.

The complementary outputs can be used when:
• additional output capability is needed for an instrument such as an oscilloscope or digital communication analyzer.
• your device requires differential inputs.

NOTE
The Generator's Data Out, Clock Out, Trigger Out and ports must be terminated with 50 Ω if they are not connected.
M8040A Generator Ports

The M8040A generator ports are used to set the generator's clock frequency and to define the output signal with respect to jitter, error insertion and signal output. In addition, the generator's output ports are also used to supply a clock signal and trigger (for example, analyzer), and an arbitrary data signal for testing your device.

The M8040A provides a high level of integration with built-in clock synthesizer, de-emphasis, jitter and level interference. It allows you to set the parameters for the built-in generator parameters such as amplifier, de-emphasis, HF and LF jitter, common mode interference and differential mode interference.

The following figure shows the M8040A generator's ports.

The M8040A generator's ports include the following:

- Remote Head - P and N Ports
  The P and N ports of each channel must be connected to the M8057A/B.

- Clk Out1 and Clk Out 2
  These are the Clk Out ports of channel 1 and 2, respectively. It can generate either a Clean Clk or all timing impairments like Data Out.

- Ref Clock In
  The Ref Clk In input can be used as reference frequency or as external system frequency directly for the instrument. An external provided signal can be measured at that input. This input is tightly involved in the system frequency generation.

- Ref Clock Out
  The Ref Clk Out is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment.
• **Clock Out and Clock Out**
  The differential clock output serve as frequency (bit rate) reference and can be set up so that they are compatible with a variety of logic families. With respect to Clock Out, **Clock Out** has inverted logic.

• **Trigger Out and Trigger Out**
  This port allows you to trigger another device (for example, an oscilloscope) and can be set up so that they are compatible with a variety of logic families. **Trigger Out** has more modes, e.g. sub rate clock to be used as ref clock for a DUT. With respect to **Trigger Out**, **Trigger Out** has inverted logic.

• **Sys Out A/B**
  The system level control outputs used to trigger events to the DUT or external instruments.

• **Ctrl Out A**
  The control output port provides the Error Output functionality.

The complementary outputs can be used when:

• additional output capability is needed for an instrument such as an oscilloscope or digital communication analyzer.

• your device requires differential inputs.

### NOTE

The Generator’s Data Out, Clock Out, Trigger Out and ports must be terminated with 50 Ω if they are not connected.

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**Understanding the Output Protection Circuit**

The M8041A and M8051A J-BERT modules offers a huge flexibility for external termination schemes and external termination voltages to address common technologies. For details, please refer to the [*M8020A Data Sheet*](#).

An internal protection circuit continuously monitors the voltages of clock, data and trigger output. It becomes active and turns off the output(s) if the externally applied termination voltage does not match the respective setting (any longer).
The M8020A/M8030A output port groups (Data, Clock and Trigger Out) have their own protection circuit. As a consequence, if an output voltage violation occurs at any of the output port(s), then the respective output port group gets disabled or stops working. The output(s) needs to be actively (via GUI or remotely) re-enabled after the fault condition has been removed.

If an output voltage violation occurs, the output(s) is switched off, which means to a “high impedance” condition. When it gets switched on again (manually by the user) it again follows the standard enabling procedure with termination voltage(s) & impedance checks.

A warning icon appears in the Status Window as shown in the following figure:

Understanding the Output Level Parameters

The following figure shows the parameters of a Data, Clock, or Trigger output signal.

As shown in this figure, the signal output levels have the following components:
• High voltage is the upper voltage level of the signal.
• Low voltage is the lower voltage level of the signal.
• Offset voltage is the offset of the average voltage level from 0 V.
• Amplitude of the signal.

When adjusting the output levels, it is important to understand the concept of how the M8020A/M8030A handles voltages.

Changing the Amplitude

Typically, during tests, when you adjust the amplitude, you want to keep the offset constant. This keeps the ideal sampling point within the eye. The M8020A/M8030A handles this by keeping offset voltage constant when amplitude is changed.

Changing the Output Levels

On the other hand, you may want to adjust the output voltage level without changing the amplitude. The M8020A/M8030A handles this by keeping amplitude constant when offset voltage is changed and high/low voltage are accordingly adjusted.

Voltage Level Restrictions

The M8020A/M8030A cannot generate a signal that has voltage levels out of range. If you try to enter a value for one parameter that would put another parameter out of limits, the M8020A/M8030A rejects the change. This could happen, for example, if low voltage is already at the minimum, and you try to lower either of high voltage or low voltage, or increase amplitude.
Understanding Delay and Crossover

The M8020A/M8030A provides the possibility of modifying the output data signal by varying the signal’s delay to the clock signal, and the signal’s crossover.

Delay

The exact time delay through a test setup can vary. The delay function allows you to compensate for this by adjusting the active edge of the trigger output relative to the clock/data outputs. This varies the phase relationship of the data and clock outputs (causes the data to have a certain time delay after the clock pulse). The higher the delay, the greater the time difference between the clock signal and the data signal. The delay can be adjusted by the generator’s Data Out 1 and Data Out 2 ports.

![Delay Diagram](image)

Crossover

Crossover is the voltage level where the overlapped rising and falling edges of the logic levels intersect. This adjustment varies the widths of the logic highs and lows.

The following figure shows examples of crossover at 50 %, 80 %, and 20 %:

![Crossover Diagram](image)

Note that the crossover feature is not supported by M8040A.
Why Incorrect Terminations Could Damage Your Device

Choosing wrong terminations may cause your device to output voltage levels that are not as expected. It may also cause excessive current or current flow in the wrong direction, which can damage your device.

Note that an internal protection circuit becomes active if the termination voltage is wrongly adjusted. The protection circuit sets the output voltages to safe levels, typically:

\[ V_{hi} = V_{lo} = V_{term} = \text{externally measured termination voltage}. \]

If you adjust the termination voltage, and try to enter value(s) which are outside of the currently allowed window, the Auto Correction Confirmation message box will pop up with respective apply and discard options as shown in the following figure:

![Auto Correction Confirmation](image)

AC Coupling and Bias Tees

The generator’s outputs are always internally DC-coupled; even when AC termination is selected. For this reason, caution must be taken when connecting your instrument to a device or test setup.

The diagram below shows a device that is AC coupled. Note that the capacitor is part of the test setup.
You can use an external bias to power your device. You must ensure, however, that the network is oriented correctly. If it is not, your device or instrument may get damaged.

The following diagram shows a bias tee that is positioned correctly. Notice that the generator's outputs are protected by the blocking capacitor.
The following drawing is an example of the external DUT connected to the generator output for the different possible settings.

This figure shows what the generator expects to be externally connected as DUT, with respect to the different selectable termination models.

For AC-coupled mode (see red box above), the instrument actually cannot and does not need to distinguish between these two termination schemes. Therefore the drop-down box **Termination Model** is not shown and active within the GUI when the AC coupled mode is selected.

There are certain impedance/voltage limits you need to keep in order to be able to turn on (enable) the output(s).

Whenever an output amplifier is turned on, the external DC resistance as well as the external termination voltage is measured and calculated.

These are the impedance/voltage limits for various modes / configurations:

- **DC Coupling Unbalanced:** The measured externally connected resistance should be within the allowed range which is between 40 to 65 Ω here. Also, if an external termination voltage is detected that is not within the allowed ±100 mV tolerance window, the output(s) will not turn on.
• **DC Coupling Balanced:** The measured externally connected resistance should be within the allowed range which is between 70 to 130 Ω here. In this DC Coupling Balanced mode there is an exception implemented, that allows the output(s) to drive high impedance ('into open'). For this, the set maximum amplitude should be below 450 mV, and the offset setting should be between 0-370 mV.

• **AC Coupling:** When using the AC coupled mode, you must apply an external DC blocking capacitor. Here the external DC resistance must be greater than or equal to 300 Ω, with the HF resistance being ~50 Ω (single-ended) or ~100 Ω (differential).

### Setting up Terminations

Before you can start sending signals to your device, you have to choose the proper termination mode. To do so:

1. Go to the **Menu Bar** > **Generator** and then select **Data Out**.
2. Select **Amplifier** functional block from the **Parameters** window.
3. Provide the DUT's termination settings.
4. Provide termination voltage.

**CAUTION**

Selecting the wrong termination may damage your device.

5. Connect the DUT's input ports to the M8020A/M8030A/M8040A's output ports.

**CAUTION**

Do not apply external voltages to the generator outputs. Output ports of the generator that are not connected to another device must be terminated with 50 Ω to prevent the M8020A/M8030A/M8040A from damage. If outputs are disconnected they are usually not turned on because the output enable check detects the misconfiguration. If outputs are disconnected after they have been turned on the protection circuit might get triggered depending on the specific configuration. In this case the output will be switched off. This is an emergency scenario and should never be a normal habit. It can be switched on again (manually by the user) after removing the fault condition, it again follows the standard enabling procedure with termination voltage(s) & impedance checks.
Setting up Generator

DC Check (Unbalanced/Balanced Termination) for M8040A

DC Check for Unbalanced Termination

**Step 1** If the Measured Voltage = VT → Pass, go to Step 2.

**Legends**
- VT – Termination Voltage
- P – Normal (Non-Inverted)
- N – Complement (Inverted)
- VCCO – Output Voltage Power Supply
- DUT – Device Under Test

**Step 2** If the Measured Voltage = VT → Pass, go to Step 3.
**Step 3** If the Measured Voltage $= VT + 50 \text{ mV} \rightarrow$ Pass, turn on the output driver.

In the above diagrams, only normal output is shown. However, the DC check however is done for normal and complement output. In general, the both outputs (P/N) need to be terminated the same way.

In single ended use case for better convenience the unused output can be terminated with 50 Ohm into GND although termination voltage of used output might not be zero. This is only true as long as the offset voltage is between +1V and -1V. The mismatch is detected during the test and is compensated internally. This is implemented in order to make the termination of unused outputs easier.
**DC Check for Balanced Termination**

**Step 1**  If the Measured Voltage = OFFSET → Pass, go to Step 2. However, this is false if DUT is unbalanced with VT unequal to OFFSET.

**Step 2**  If the Measured Voltage = OFFSET + 100 mV → Pass, go to Step 3. However, this is false if DUT is unbalanced (no matter if VT is equal or unequal to OFFSET).
Step 3  If the Measured Voltage for P is OFFSET +50 mV and for N is OFFSET -50 mV → Pass. Turn on the output driver. However, this is false if DUT is not connected or AC coupled.

Adjust Output Levels (optional)

Data, Clock and Trigger Out offset and voltage levels can be adjusted. This is typically done when you want to tune your BER measurement or stress the device.

You can adjust the related parameters of the data and clock amplitudes and offsets on the GUI.

To enter specific values for the outputs from the keyboard:
1 Go to the Menu Bar > Generator and then select Data Out and Trigger Out ports. Once more, go to the Menu Bar > Generator and then select Clock Out port.
2 Select Amplifier functional block from the Parameters window.
3 Select coupling as DC.
4 Select termination model as Unbalanced.
5 Enter the desired termination voltage.
De-Emphasis Signal Generator

The M8020A/M8030A has a built-in de-emphasis signal generator that can be connected between the Data Out port of the generator and the DUT.

De-emphasis is a method that reduces the voltage of a digital signal if the generated level is high or low for more than one clock period. The principle is illustrated in the following figure.

The de-emphasis amplitude is specified as a fraction of the output amplitude (in percent or dB).

**Post-cursor de-emphasis**

The figure above refers to a so-called post-cursor de-emphasis. You may wish to know how that is generated.

- One branch has a programmable amplifier to produce the desired output voltage (Peak to Peak Voltage).
The other one has an adjustable delay (automatically set to one signal clock period) and a programmable inverting attenuator/amplifier to produce the delayed signal with a lower voltage swing. Finally, the signals of both branches are added. This means, the delayed signal voltage is subtracted from the specified peak-to-peak amplitude.

**Pre-cursor de-emphasis**

It is also possible to convert the input signal to a pre-cursor deemphasized signal.

This can be done by setting the output voltage swing to the desired deemphasis amplitude and specifying a negative amplitude ratio (an amplification). This inverts the roles of the two branches. The delayed signal has now a larger amplitude than the direct signal. A waveform example is illustrated in the following figure.

When pre-cursor de-emphasis is generated this way, the complementary Output of the De-Emphasis Signal Converter becomes the normal output and vice versa.

**CAUTION**

Be very careful if you set the de-emphasis ratio to amplification! In this case, there is no indication of the peak-to-peak voltage applied to the DUT. You need to calculate or measure the output signal voltage precisely. Otherwise you might damage your device.
De-emphasis on 2 pre-cursor and 5 post-cursors

The following example illustrates the output of the differential signal with variable de-emphasis on 2 pre-cursor and 5 post-cursors generated by M8020A/M8030A De-Emphasis.

Controlling the De-Emphasis

To control the de-emphasis function:
1. Go to the Menu Bar > Generator and then select Data Out.
2. Select De-Emphasis function block from the Parameters window.

For M8020A/M8030A, you have two (pre-cursor) and five (post-cursor) and the corresponding unit.
You can use the **Preset Enable** button to enable/disable changing the de-emphasis preset register number. Once the **Preset Enable** option is enabled, you can set the preset register number. There are 31 preset registers available addressed by a register index of 0 up to 30. The tap values of the ‘current’ preset register are shown at the output. Preset register 0 is the default register. Supported preset values for M8041A, M8051A and M8062A are 0 - 30 and for M8061A, the only preset value is 0.

You can toggle between dB (decibel) and % (percent). Toggling does not change the value. The **De-Emphasis** function block also allows you to set the “Positive” or “Negative” polarity for de-emphasis.

**M8045A De-Emphasis**

The M8045A provides built-in 5 taps de-emphasis with positive and negative cursors based on a finite impulse response (FIR) filter. You are allowed to enter the de-emphasis values in terms of coefficient values. You can set the two post-cursor, main cursor and two pre-cursor by adjusting the coefficient values.
Setting up Generator

Controlling the M8045A De-Emphasis

To control the M8045A de-emphasis function:

1. Go to the **Menu Bar > Generator** and then select **Data Out**.
2. Select **De-Emphasis** function block from the **Parameters** window. The following **De-Emphasis** parameters will be shown:

```
Table 48 Specifications for multi-tap de-emphasis

<table>
<thead>
<tr>
<th></th>
<th>NRZ</th>
<th>PAM4</th>
</tr>
</thead>
<tbody>
<tr>
<td>De-emphasis taps</td>
<td>5 taps, can be adjusted for each channel independently</td>
<td></td>
</tr>
<tr>
<td>Coefficient 0</td>
<td>0.0 to ± 0.4</td>
<td>0.0 to ± 0.4</td>
</tr>
<tr>
<td>Coefficient 1</td>
<td>0.0 to ± 0.4</td>
<td>0.0 to ± 0.4</td>
</tr>
<tr>
<td>Coefficient 2 (Main)</td>
<td>0.0 to 1.0</td>
<td>0.0 to 1.0</td>
</tr>
<tr>
<td>Coefficient 3</td>
<td>0.0 to ± 0.45</td>
<td>0.0 to ± 0.45</td>
</tr>
<tr>
<td>Coefficient 4</td>
<td>0.0 to ± 0.45</td>
<td>0.0 to ± 0.45</td>
</tr>
<tr>
<td>Cursor coefficient resolution</td>
<td>0.01</td>
<td>0.01</td>
</tr>
</tbody>
</table>
```
For M8045A, you have two pre–cursor (Coefficient 1 and 2), two post–cursor (Coefficient 3 and 4), one main–cursor (Coefficient 2) and the corresponding unit. You can enter the de–emphasis values in terms of coefficient values. Once you enter the coefficient values, the pre–cursor and post–cursor values are automatically reflected in the corresponding fields. Once the Automatic Main–Cursor button is enabled, you are not allowed to adjust the main cursor as it is automatically calculated. However, to change the values for main cursor, you need to disable the Automatic Main–Cursor button. You are allowed to toggle between dB (decibel) and % (percent). Toggling does not change the value.

Set the values as following:

- **Automatic Main–Cursor button**: Enables automatic calculation of the main cursor.
- **Coefficient 0**: Controls the filter coefficient 0.
- **Coefficient 1**: Controls the filter coefficient 1.
- **Coefficient 2 (Main)**: Controls the filter coefficient 2 (main cursor).
- **Coefficient 3**: Controls the filter coefficient 3.
- **Coefficient 4**: Controls the filter coefficient 4.
- **Output Swing**: Resulting peak to peak output swing as percentage of the configured output amplitude.
- **Unit**: You can toggle between dB (decibel) and % (percent).

Here are the formulas to calculate decibel values from the cursor magnitude values:

- c0: Coefficient 0
- c1: Coefficient 1
- c2: Coefficient 2
- c3: Coefficient 3
- c4: Coefficient 4

Pre–Cursor2: \(20 \times \log\left(\frac{c_0-c_1-c_2-c_3-c_4}{-c_0-c_1-c_2-c_3-c_4}\right)\)

Pre–Cursor1: \(20 \times \log\left(\frac{c_0+c_1-c_2-c_3-c_4}{c_0-c_1-c_2-c_3-c_4}\right)\)

Post–Cursor1: \(20 \times \log\left(\frac{c_0+c_1+c_2+c_3-c_4}{c_0+c_1+c_2-c_3-c_4}\right)\)

Post–Cursor2: \(20 \times \log\left(\frac{c_0+c_1+c_2+c_3+c_4}{c_0+c_1+c_2+c_3-c_4}\right)\)
M8040A Automatic Pattern Generator De-emphasis

The Auto De-emphasis feature optimizes the de-emphasis settings at the end of the cable to get the best eye performance from the instrument. Additionally, this feature allows you to de-embed/embed cable or fixture using an s-parameter file.

Connection Diagrams

Connection Diagram 1

The following figure shows how to establish a connection among M8045A, M8057A/B and 86100D with 86108B:
Connection Diagram 2

The following figure shows how to establish a connection among M8045A, M8057A/B and N1000A with N1060A:
Connection Diagram 3

The following figure shows how to establish a connection among M8045A, M8057A/B and N1094A:

Connection among M8045A, M8057A/B and N1094A

Using FlexDCA from within M8070B

For details on controlling FlexDCA (86108B/N1060A/N1094A/N1094B) from M8070B, refer to M8070ADVB Advanced Measurement Package User Guide or Online Help.
Controlling M8040A Automatic Pattern Generator De-emphasis

1. To control the M8045A auto-deemphasis function, do the following:
   a. Go to the Menu Bar > Generator and then select Data Out.
   b. Select Deemphasis function block from the Parameters window.

   The following Deemphasis parameters will be shown:

   ![Deemphasis parameters screenshot]

   c. Set the Deemphasis values as following:
      - **Oscilloscope Channel**: Select a channel to perform the auto deemphasis, and then click Execute button.
      - **Automatic Main-Cursor** toggle button: Enables automatic calculation of the main cursor.
      - **Coefficient 0**: Controls the filter coefficient 0.
      - **Coefficient 1**: Controls the filter coefficient 1.
      - **Coefficient 2 (Main)**: Controls the filter coefficient 2 (main cursor).
      - **Coefficient 3**: Controls the filter coefficient 3.
      - **Coefficient 4**: Controls the filter coefficient 4.
      - **Output Swing**: Resulting peak to peak output swing as percentage of the configured output amplitude.
      - **Unit**: You can toggle between dB (decibel) and % (percent).
2 The embedding process enables to add the S21 loss to the de-emphasis tap settings within the given de-emphasis tap resolution/range. To control the Embedding function, do the following:
   a  Select Embedding function block from the Parameters window.
   The following Embedding parameters will be shown:

   ![Embedding Parameters](image1)

   b  Set the Embedding values as following:
      - **State**: Enables/Disables S-Parameter compensation.
      - **S-Parameter Profile**: Selects the S-Parameter profile. It also allows you to import and export a S-Parameter profile. It supports S2P file format for Embedding.

3 The de-embedding process enables to compensate the loss of cable or channel using the generators de-emphasis capability with the given resolution/range. To control the De-Embedding function, do the following:
   a  Select De-Embedding function block from the Parameters window.
   The following De-Embedding parameters will be shown:

   ![De-Embedding Parameters](image2)

   b  Set the De-Embedding values as following:
      - **State**: Enables/Disables S-Parameter compensation.

---

**NOTE**

The auto deemphasis adjustment is supported only for NRZ and PAM4 Line Coding.
### Setting up Generator

- **S-Parameter Profile**: Selects the S-Parameter profile. It also allows you to import and export a S-Parameter profile.

### Setting Up Data Out Port Parameters

The generator produces clock and data outputs that serve as frequency reference and device stimulus for the device under test.

To set the Data Out parameters:

1. Go to the **Menu Bar > Generator** and then select **Data Out** port.
2. Select **Amplifier** functional block from the **Parameters** window.
3. Set the parameters as described in this section.

#### Amplitude

This text field allows manual entry of the voltage amplitude and displays the current value.

To modify the value, click inside the text field and enter the desired value.
You can even click **Auto Range** option which will automatically select the amplitude range according to amplitude.

**High Voltage**

This text field allows manual entry of the logic high voltage level and displays the current value.

To modify the value, click inside the text field and enter the desired value.

**Offset Voltage**

This text field allows manual entry of the voltage level halfway between logic high and logic low (the offset) and displays the current value.

To modify the value, click inside the text field and enter the desired value.

**Low Voltage**

This text field allows manual entry of the logic low voltage level and displays the current value.

To modify the value, click inside the text field and enter the desired value.
Crossover

This text field allows manual entry of the data’s crossover percentage, and displays the current value.

Note that the crossover feature is not supported by M8040A.

Clk/2 Jitter

This text field allows manual entry of the Clk/2 Jitter at the Data Out port in units of seconds. It provides half rate clocking; the clock at the clock output runs at half the bit rate.

Data Polarity Inverted

Use this option to invert the logic of the data outputs (Data Out, Trigger Out and Clock Out).

Transition Time

Use this option to control the transition time of the output signal. The choices are smooth, moderate and steep.

Note that the transition time is not supported by M8040A.

Setting up Output Timing

The Output Timing functional block provides the following parameters:

- **Data Rate** - Sets the channel data rate in b/s. To set up the data rate, go to Clock Generator and set the Frequency.
- **Delay** - Controls the data delay of the output signal. This also affects the channel’s Clock Out signal when the clock source is configured as Data Clock.
Setting up Generator

- **Jitter Delay** - Controls the delay of jitter profile. Use this option to adjust the jitter phase between multiple outputs (e.g. clock and data) on the receiving side to ensure error-free sampling for the jitter frequencies and amplitudes used in the setup.

- **Deskew** - This feature is used to match or adjust the timing delay between the Data Out channels. It is a delay offset that is intended to deskew the output in respect to other outputs. This value is an offset to the data delay as well as jitter delay.

**Line Coding**

You can define the line coding for a Data Out port of the M8045A, M8195A and M8196A modules through the Parameters window.

To set the line coding:

1. Go to the Menu Bar > Generator and then select Data Out.
2. Select Line Coding functional block from the Parameters pane.
3. Select the line coding.

   - For M8195A and M8196A modules, the Data Out port supports NRZ and PAM-4 line coding which defines how consecutive data bits are mapped to symbols.

   ![Line Coding](image1.png)

   For M8045A module, the Data Out port supports NRZ, PAM-3, and PAM-4 line coding.

   ![Line Coding](image2.png)
The PAM-3 line coding provides the Symbol Level options which controls the PAM-3 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM-3 symbol. The levels of PAM-3 symbol 0 and 2 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.

The **PAM-4** line coding provides the following symbol mapping options:

- **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 10 maps to symbol 2 and 11 maps to symbol 3.
- **Gray Coded** - In this mapping, the bit sequence 00 maps to symbol 0, 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.
- **Custom** - In this mapping the consecutive data bits are mapped to symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10). The position within this list corresponds to the symbol level. First value is for Symbol 0 and the last value is for Symbol 3.
• **Symbol Level**: It controls the PAM4 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM4 symbol. The levels of PAM4 symbol 0 and 3 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.

**NOTE**

Make sure to use the similar line coding for all Data Out ports of M8045A/M8195A/M8196A. An "Auto Correction" window will appear if you select different line coding for Data Out ports. Clicking on the "Allow" button, present on this window applies same line coding on all Data Out ports.
Bit Rate

Bit rate is defined as bits per second. The Generator’s clock rate sets the bit rate and serves as the frequency reference for the Data, Clock and Trigger outputs, your device, and the Analyzer (if it receives its clock from the Generator). It can be generated internally or supplied from an external source.

When to Use an External Clock Source?

The M8020A/M8030A/M8040A’s internal clock can be used for most testing purposes.

There are some circumstances, however, when an external clock source is required:

- Synchronization with an external clock
  The M8020A/M8030A/M8040A can be connected to an external clock to allow it to run as part of a larger external system.
- Use of a modulated clock
  A frequency- or delay-modulated clock can be used to provide a small amount of jitter to the clock signal.
- Use of a precision clock
  A precision clock with very low phase noise can be used to enhance the instrument’s performance. This is especially interesting for long term measurements.

Bit Rate Range

The M8040A provides symbol rate from 2.0 to 32.4 Gbaud for M8045A Option -G32 and 2.0 to 58.0 Gbaud (all specifications are valid up to 58 Gbaud with over-programming up to 64.8 Gbaud) for M8045A Option -G64.

The M8020A/M8030A provides bit rates from 256 Mbit/s up to 16.2 Gbit/s, depending on the instrument’s options.

However, several specific properties and limitations need to be taken into account when working at low bit rates. The limitations apply to the instrument according to the following hysteresis curve:

- If the bit rate falls below 615 Mbit/s, the limitations apply.
- If the bit rate exceeds 620 Mbit/s, the limitations no longer apply.
The following figure clarifies the behavior in the range between 615 Mbit/s and 620 Mbit/s:

For the generator the following rules apply:
- Below 620 Mbit/s, the Generator can only be operated with an external clock source, because the internal clock source can only produce signals higher than 620 Mbit/s.
- The trigger output cannot be set up to trigger on certain pattern positions or pattern sequences. If this option is enabled (for example in the user interface), the trigger is sent once for each pattern, but the bit position cannot be specified.
  The option to trigger on the divided clock signal is supported as usual.
- There are restrictions to the available clock to data delay values.
  The Generator can vary the clock to data delay only within a range of 10 ns (relative to the clock signal). For frequencies above 666 Mbit/s, this range is sufficient to cover the complete clock cycle (= 1 unit interval).
  For lower frequencies, the valid data delay range is smaller than the clock cycle. The Generator cannot generate signals with a delay outside this range. Therefore, the data delay cannot be set to all values within the clock cycle.
Spread Spectrum Clocking

A Spread Spectrum Clock (SSC) is widely used for reducing the peak electromagnetic radiation at the nominal clock frequency. With SSC, the clock pulse is modulated with a relatively low-frequency triangle waveform. This broadens the clock signal spectrum and reduces the peak energy. The M8020A/M8030A allows to emulate such SSC on the data, trigger and clock output signals.

The M8020A/M8030A has a built-in SSC generator.

For the SSC settings, go to Menu Bar > Clock > Clock Generator and then select SSC function block from the Parameter window.
Setting the Bit Rate

You can use an external clock source or the M8020A/M8030A/M8040A's internal clock to control the bit rate.

To set the bit rate:

1. Go to **Menu Bar** > **Clock** and then **Clock Generator**.
2. Select **Synthesizer** function block from the **Parameter** window.
3. Select the appropriate clock source from the following options:
   - **Internal** - When clock source is selected as Internal, an internal clock oscillator is used. For the internal clock source, different reference clock sources are available for the internal oscillator. When the Reference frequency is selected as Internal 100 MHz, then 100 MHz Reference clock of M8041A/ M8045A module is used and when Reference frequency is selected as AXIe 100 MHz, then 100 MHz reference clock of M950XA AXIe chassis is used.
   - **Reference** - To use clock source as Reference, we need to connect external reference clock source to Ref Clk In port of M8041A/ M8045A module. Depending upon the connected clock source, you have to choose between either 100 MHz reference frequency or 10 MHz reference frequency.
   - **Direct** - To use Clock source as Direct, you need to connect external clock source to Ref Clk In port of M8041A/ M8045A port. Enter the frequency of the clock source as the Reference frequency. Also, you can use the **Execute** button to measure the frequency of the connected clock source. This connects the external clock directly to the clock generator at 8.1 GHz to 16.20 GHz.
   - **Clock Multiplier** - To use the clock source as Clock Multiplier, you need to connect external clock source to the Ref Clk In port of the M8041A/ M8045A module and then specify the reference frequency. You can generate the specific frequency by choosing multiplier and divider value. Also, you can use the **Execute** button to measure the frequency of the connected clock source. The Clock Multiplier option is also supported by M8045A. This option can be enabled by...
using the M8045A-0G6 license. For more details on licensing, refer to M8040A Licenses on page 557. This option is applicable for PCIe 2.5G, 5G, 8G, and 16G. To use the clock multiplier feature in M8040A, the serial number of M8045A module must be greater than or equivalent to 1000.

4 For Direct clock source, click **Execute** button to measure the incoming clock’s clock rate.

5 Select a clock rate:
   - For Internal Clock Source, you can enter a clock rate in the Value and Units field.
   - For 10/100 MHz Ref Clock Source, the clock connected to the 10/100 MHz Ref In port must be 10/100 MHz.

The selected clock rate applies to the generator. This is also the clock rate generated at the generator’s Clock Out port.

The analyzer internally receives its clock from the generator, it runs at the same clock rate.

**External Clock Divider**

The internal clock (i.e. the bitrate) is the external clock divided by the value specified in the clock divider field. The external clock divider field is available if you have close an external clock source.

**External PLL Clock Divider and Multiplier**

The internal clock (i.e. the bitrate) is the external PLL divided by the value specified in the divider field and multiplied with the value specified in the multiplier field. The external PLL clock divider and multiplier field are available if you have chosen a clock source.

**Clock Rate Indicators**

The Bit Rate indicators are shown in the **Status Indicators** display their current bit rate.

The analyzer bit rate is measured from the incoming clock signal or derived from the data signal.
Trigger Output

The generator’s Trigger Out port can be used to send a trigger to external devices like an oscilloscope or digital communication analyzer.

In pattern mode, the generator sends a trigger signal that is at least 32 bits long.

In sequence mode, the generator can send a trigger signal whenever a block of the sequence starts or restarts.

Several options are available for the trigger signal. As an example, you can send the trigger as a divided clock signal or as an indicator when the data pattern starts.

Setting Up Trigger Output

To set up the generator’s Trigger Output port:
1. Connect the external instrument to the Trigger Out port.
2. Go to Menu Bar > Generator > and then select Trigger Out.
3. Provide the necessary configuration.

The delay option in the Trigger Out functional block sets the delay of the trigger output. When it is set to 0 ps, this means there is no delay or the trigger output and data output are in sync. When it is set as 10 ps, this means the signal which will be received at trigger output port will have a delay of 10 ps.

You can always generate a divided clock signal at the Trigger Out port.

The alternate trigger signals refer to patterns and are not generated in sequence mode.

If SSC is enabled, then it also have impact on trigger output signal.

To support the generation of a trigger spike at the beginning of a sequence block, the Trigger Output can be put into Sequence mode.

**NOTE**

The jitter at Trigger Out is always the same as jitter at Clock Out. Since, there are no parameters available in the M8070B GUI to set jitter at Trigger Out, it can be set using Clock Out parameters.
Clock Divided by \( n \)

Select this option to send a trigger signal from the Trigger/Ref Clock Out port at every \( n \)th clock pulse. Note that the trigger signal itself consists of \( n/2 \) bits high followed by \( n/2 \) bits low. For example, Clock divided by 8 works as shown below.

![Clock and Trigger Out signal](image)

**NOTE**

If the Divider Factor \( n \) is uneven (for example, 3), the clock's duty cycle will not be 50%, but the signal will stay high for \((n+1)/2\) and low for \((n-1)/2\). This results in a Duty Cycle Distortion (DCD) of 0.5 UI.

Sequence Trigger

This function becomes available after a user-defined sequence has been downloaded to the generator.

Click this function to switch the Trigger Out port to Sequence mode.

In Sequence mode, the Trigger Out can generate a spike whenever the execution of a block starts or restarts. Whether that happens for a particular block or not is defined for each block individually in the sequence expression.
Error Insertion

To test error correction algorithms, alarms and other functions that are embedded in the data pattern, you can insert logic errors (flipped bits) into the pattern.

For the error insertion, go to Menu Bar > Data Out and select Error Insertion function block from the Parameters window.

The instrument provides several options for inserting error bits manually or automatically. You have the following options for inserting errors into the output data stream:

Insert Single Bit Stream

To insert single bit stream:

- Click the slide switch to turn on the Error Insertion state.
- Select the supported mode from the drop-down list.
- Select the error ratio from the drop-down list.

Insert Single Bit Error

- To manually insert a single bit error into the output stream:
  - Click the Data Out port.
• Select Error Insertion functional block and enable the Insert Single Bit Error state.
• Click Execute.

**NOTE**

TIP - To find out how your DUT reacts on very small bit error rates, set up the pattern generator to enter errors once every $10^{-12}$ bits and run a longer accumulative test.

You can then find the DUT's true error rate by calculating the difference between the bit error rate set up in the Generator and the accumulated bit error rate found by the Analyzer.

**NOTE**

If you set up too high an error rate, the Analyzer will not be able to synchronize to the incoming pattern. When setting up an error rate, always make sure that the synchronization threshold is higher than the bit error rate.
FEC Error Insertion

The FEC error insertion is independent from the error insertion controlled with the **FEC Error Insertion** functional block available in the **Parameters** window. Both error insertions can be used at the same time.

The FEC error insertion is a license feature and is supported by M8070B software by installing a module specific FEC license. For details on FEC license, please refer to the **M8040A Licenses** on page 557.

FEC is enabled by selecting one of the FEC factory patterns.
- IEEE_802_3cd_RS_544_514_Scrambled_Idle
- IEEE_802_3cd_RS_544_514_Remote_Fault

To generate FEC for PAM4 on M8045A, follow the given steps using M8070B **Setup View** as illustrated in the following figure:
1. On the **Clock Generator** functional block, set the symbol rate between 16.208 GBd to 26.563 GBd. Please note that the FEC engine only supports 26.5625 GBd PAM4 signals.

2. On the **Data Out** functional block, set output levels. Make sure to turn **ON** the output levels.

3. On the **Line Coding** functional block select **PAM4**. Enable the PAM4 **Pre-Coder**. Enabling the pre-coder is optional and is only required if the DUT also have the pre-coder enabled.

4. Next step involves selecting the FEC pattern. To do this, click **Select Pattern** dialog. For more information on this dialog, refer to **Select Pattern Dialog** on page 420. Use this dialog to download FEC pattern on the **Data Out** locations as shown in the following figure:

Both channels of the M8045A generate the FEC encoded signal independently. When setting up the same sequence for both channels, both channels will generate the exactly same bit sequence.

5. The FEC pattern will be now available in the **Sequence Editor**. Infinitely loop the PRBS, FEC encoded scrambled idle and FEC remote fault patterns. Press the Break button to move the sequence to the next block. Refer to **Sequence Editor** on page 389 for details on how to create, loop and break sequences.
FEC patterns require a block length of 5440 and use either an infinite loop or counted loop. The loop count must be a multiple of 8.
Due to the differences between FEC frame length and sequencer word width, there will be phases of invalid FEC data when transitioning from a FEC encoded sequence lock into a non-FEC sequence block and vice versa.

6 You can now insert the FEC error into the output data. It can be either pre-FEC error or post FEC error. Select **FEC Error Insertion** function block from the **Parameters** window.
You have the following options for inserting FEC errors into the output data stream:

- **State** - Enables/disables the continuous FEC error insertion. The inserted errors are after the FEC encoding.
- **Errors per Frame** - Specifies the number of symbols to be corrupted within a single FEC frame. The inserted errors are at random symbol positions. Each corrupted symbol will contain exactly one bit error at a random bit position.
- **Insert Single BIP Error** - Insert a single Bit Interleaved Parity (BIP) error. This is a pre-FEC error and can be inserted at any time, even if the FEC error insertion is disabled.

### FEC Remote Programming

The following SCPI commands can be used for FEC error insertion remote programming:

1. Commands for selecting FEC patterns:
   
   ```
   :DATA:SEQUence:SET 'M1.DataOut1',Memory,'factory:FEC/IEEE_802_3cd_RS_544_514_Scrambled_Idle'
   ```

2. Commands for FEC error insertion:
   
   a. Enable/disable symbol error insertion
      
      ```
      :DATA:FEC:EINSertion:STATe 'M1.DataOut1',<0|1|OFF|ON>
      ```
   
   b. Set the number of symbol errors per FEC frame
      
      ```
      :DATA:FEC:EINSertion:ERRors 'M1.DataOut1',<NR1>
      ```
   
   c. Insert a single BIP error
      
      ```
      ```

For further details on these SCPI commands, please refer to the *M8000 Series Programming Guide*. 
Interference

The M8020A/M8030A supports the following two types of interference:
- Common Mode Interference (CMI)
- Differential Mode Interference (DMI)

Common Mode Interference (CMI)

Common Mode Interference (asymmetrical mode) relates to ground (CMI). It has the following characteristics:
- **State**: Enables / disables common mode interference (CMI).
- **Amplitude**: Specifies the amplitude of the common mode interference (CMI).
- **Frequency Source**: Specifies the frequency source for common mode interference (CMI). It can be high frequency source or low frequency source.
Differential Mode Interference (DMI)

Differential Mode Interference (DMI) - Differential Mode Interference (symmetrical mode) is independent of ground (DMI). It has the following characteristics:

- **State**: Enables / disables differential mode interference (DMI).
- **Amplitude**: Specifies the amplitude of the differential mode interference (DMI).
- **Frequency Source**: Specifies the frequency source for differential mode interference (DMI). It can be high frequency source or low frequency source.
- **High Frequency**: Specifies the frequency of the high frequency source.
- **Low Frequency**: Specifies the frequency of the low frequency source.
Jitter Setup

The Jitter Setup function is used for composing the total jitter in a defined and calibrated way.

The M8020A/M8030A/M8040A supports the following types of jitters:
- High Frequency Jitter (HF Jitter)
- Low Frequency Jitter (LF Jitter)

High Frequency Jitter (HF Jitter)

The High Frequency Jitter is a composition of the following types of jitters:
- Periodic Jitter 1
- Periodic Jitter 2
- Bounded Uncorrelated Jitter
- Random Jitter
- Spectrally Distributed Random Jitter
- External Jitter Source (Connected to the Delay Ctrl input)

Low Frequency Jitter (LF Jitter)

The Low Frequency Jitter is a composition of the following types of jitters:
- Periodic Jitter 1
- Periodic Jitter 2
- Residual Spread Spectrum Clock

How to Enable Global Jitter State

You can enable the global jitter state by selecting the Enable Impairments check box, present on the status bar of the GUI.
Set Jitter Configuration

In this section, an example of Periodic Jitter 1 is shown to specify the jitter components.

To specify the jitter components:
• **Set Unit**: Defines the unit of jitter amplitude value in either seconds or UI.
• **Set Delay**: Enter a value to define the jitter delay on clock and data.
• **Enable Jitter**: Enable the jitter source (press the corresponding button).
• **Set Parameters**: Set the most commonly used parameter (typically Amplitude and Frequency) directly.

![Jitter Configuration Interface]

Spread Spectrum Clock

The Spread Spectrum Clocking setting controls the generator’s spread spectrum (SSC) clocking feature. When the SSC is enabled, it impacts the Data Out, Clock Out, and Trigger Out ports.

The spread spectrum clock is characterized by:
• Deviation
• Frequency
• Type
• Profile
• Shape
• Deviation

If the deviation type Center Spread is selected, the deviation can be changed in two different ways:

- **Change the Center Spread value**: the bit rate remains unchanged, while the upper and lower frequency changes according to the selected deviation. The deviation value specifies $\frac{1}{2}$ p-p value.

- **Change the Down Spread value**: the upper frequency remains unchanged, while the bit rate is adjusted. The deviation value specifies the p-p value.

For some setups, the I/Q modulator’s range limitations require to use Center Spread instead of Down Spread and adjust the bit rate (and deviation) accordingly.

If the upper or lower frequency is change, the bit rate will be adjusted according to the selected deviation. The center frequency corresponds to the configured bit rate.

Please note that both the upper and lower frequency and the frequency adjustment of all three frequencies are not reflected in the firmware. The GUI just calculates the resulting bit rate and writes it to the firmware.

The **Deviation** of the clock rate. The ranges of SSC deviation are as follows:

- Down Spread with deviation of 0 ... 1 PPM
- Up Spread with deviation of 0 ... 1 PPM
• Center Spread with deviation of 0 ... 1 PPM
• Asymmetric allows to independently specify up and down deviation. When this is selected, the deviation is no longer specified in terms of peak-peak deviation, but independently for up and down deviation. The value ranges for the up deviation are 0 PPM to 1 PPM and for down deviation are -1 PPM to 0 PPM. The Asymmetric deviation type is only available in M8041A and M8046A modules.

The deviation in Upspread and Downspread is the p-p value while in Centerspread it is 1/2 p-p.

**NOTE**

- **Frequency**: The deviation Frequency. The SCC provides the frequency range of 100 Hz – 200 kHz.
- **Type**: You can click the drop-down list to choose among Down Spread, Up Spread, Center Spread and Asymmetric deviation type.
- **Profile**: Controls the profile of the spread spectrum clocking. You can use the drop-down list to choose between the Triangular and Arbitrary profile.
- **Shape**: For Arbitrary profile, you need to specify the Arbitrary Waveform file. It is a simple text file that contains the data points which define the arbitrary waveform of the SSC profile.

### Periodic Jitter 1

The **Periodic Jitter 1** is characterized by:

- Amplitude
- Frequency
5 Setting up Generator

- **Amplitude**: Controls the amplitude of periodic jitter 1.
- **Frequency**: Controls the frequency of the periodic jitter 1.

### Periodic Jitter 2

The **Periodic Jitter 2** is characterized by:

- **Amplitude**
- **Frequency**

### Specify the Components for Jitter Sweep

The **Periodic Jitter 2** has the following modes:

- Constant Amplitude Sweep
- Variable Amplitude Sweep

To specify the components of jitter sweep select **Jitter Sweep** functional block from the **Parameter** window and then select the **Mode** from the drop-down list to specify components the jitter sweep.
**Periodic Jitter 2 – Constant Amplitude Sweep Parameters**

The **Periodic Jitter 2 – Constant Amplitude Sweep** is characterized by:

- **Amplitude**: The maximum peak-to-peak Amplitude is limited by the free capacity of the chosen delay line.
- **Frequency Range**: The stop frequency has to be higher than start frequency and the range should be in accordance with the selected waveform.
- **Sweep Time**: You can specify the duration for sweeping the specified frequency range once.
- **No. of Steps**

![Jitter Sweep](image)

- **Amplitude**: The maximum peak-to-peak Amplitude is limited by the free capacity of the chosen delay line.
- **Frequency Range**: The stop frequency has to be higher than start frequency and the range should be in accordance with the selected waveform.
- **Sweep Time**: You can specify the duration for sweeping the specified frequency range once.
• **No. of Steps**: You can specify the number of steps to fulfill a complete sweep. The start and stop values are included. The valid range is between 2 to 100.

**Periodic Jitter 2 – Variable Amplitude Sweep Parameters**

The **Periodic Jitter 2 – Variable Amplitude Sweep** is characterized by:

- Standard
- Sweep Time
- No. of Steps
- Step Distance

- **Standard**: You can use this drop-down list to specify whether you want to select a pre-defined standard or a user-defined standard. All the available predefined standards will be shown in this list. However, if you select the user-defined standard, press **Jitter Profile** button to locate the **Jitter Tolerance** standard. The user-defined standard uses the same file format like the **Jitter Tolerance Compliance** measurement.
Selecting the Standard does allocate the required amount of jitter modulation on the delay line being used. To avoid errors when changing the selection, it is recommended to either select the corresponding bit rate first, or enable the PJ2 source after setting the correct bit rate.

- **Sweep Time**: You can specify the duration for sweeping the selected jitter profile/standard once.
- **No. of Steps**: You can specify the number of steps to fulfill a complete sweep. The start and stop values are included. The valid range is between 2 to 100.
- **Step Distance**: You can use this drop-down list to specify whether the frequency steps are log equidistant (EQUidistant) along the periodic jitter curve or a frequency step matches a corner frequency on the periodic jitter curve.

**Bounded Uncorrelated Jitter**

**Bounded Uncorrelated Jitter** is characterized by

- Amplitude
- PRBS polynomial
- Data rate
- Filter type

- **Amplitude**: Controls the amplitude of the BUJ jitter source.
• **PRBS polynomial**: The PRBS polynomial can be chosen from a list. Available are eight polynomials, from $2^7-1$ up to $2^{31}-1$.

• **Data Rate**: Enter an appropriate **Data Rate**.

• **Filter Type**: The bounded uncorrelated jitter source is equipped with three low-pass filters with cut-off frequencies at 50, 100, and 200 MHz. One of these filters is always active.

### Random Jitter

**Random Jitter** is characterized by:

- **Amplitude**
- **Filter Settings**

![Random Jitter Settings](image)

- **Amplitude**: The random jitter Amplitude must be entered as an rms (root mean square) value.

- **Filter**: The random jitter source is equipped with a 10 MHz high pass and a 100 MHz, 500 MHz and 1 GHz low pass filter to limit the spectral range.

**NOTE**

Please note that the minimum data rate must be set 8 GHz in order to set the RJ low pass filter to 1 GHz.
Spectrally Distributed Random Jitter

Spectrally Distributed Random Jitter is composed of two jitter sources: low frequency jitter and high frequency jitter. It is characterized by the amplitudes of the low and the high frequency jitter.

The sRJ on M8045A requires M8045A-0G3 license.

Spectral Distributed Random Jitter is characterized by

- Amplitude LF
- Amplitude HF

It has the following parameters:

- **sRJ State**: Click this switch to enable the spectrally distributed random jitter.
- **SRJ Amplitude 1 (RMS) LF**: This is the low frequency jitter amplitude as rms value.
- **SRJ Amplitude 2 (RMS) HF**: This is the high frequency jitter amplitude as rms value.
- **sRJ Low Pass Filter**: The spectrally distributed random jitter is equipped with a 100 MHz low pass filter to limit the spectral range, which can be enabled by pressing the corresponding switch.
Residual Spread Spectrum Clock

The Residual Spread Spectrum Clock (rSSC) is generated by modulating the clock that is used for data generation.

The Residual Spread Spectrum Clock is characterized by:
- rSSC Amplitude
- rSSC Frequency

It has the following parameters:
- **rSSC State**: Click this button to enable/disable the Residual Spread Spectrum Clock.
- **rSSC Amplitude**: This is the amplitude of the rSSC jitter source.
- **rSSC Frequency**: This is the frequency of the rSSC jitter source.

External Jitter Source

To enable the external jitter source:
- From the Data Out port select HF Jitter functional block in the Parameters window.
- Click the External switch to enable external jitter.

**NOTE**

Even if the external jitter source is enabled, you can still add or change internal jitter components.
The **TxEQ Matrix Editor** enables you to either create a new TxEQ coefficient matrix or modify an existing matrix to support PCIe de-emphasis values.

**Launching the TxEQ Matrix Editor**

To launch the **TxEQ Matrix Editor** from the M8070B application, follow one of the following procedures:

- Launching the TxEQ Matrix Editor through M8070B Menu Bar
- Launching the TxEQ Matrix Editor through M8070B Module View Parameters Window

**Launching the TxEQ Matrix Editor through M8070B Menu Bar**

**Prerequisites**

- The PG module must be connected
- The PCIe LTSSM licenses must be installed
To launch the TxEQ Matrix Editor through M8070B Menu Bar, perform the following steps:

- Go to Menu Bar > Generator > TxEQ Matrix Editor.

The **PCle TxEQ Matrix Editor - Untitled Matrix** window appears.
Launching the TxEQ Matrix Editor through M8070B Module View Parameters Window

Prerequisites

- The PCIe option must be selected under the PHY Protocol drop-down list in the Sequence Configuration parameter. For more information, refer to M8046A PHY Protocol Selection (SKP OS Filtering).

To launch the TxEQ Matrix Editor through M8070B Module View Parameters window, perform the following steps:

1. Go to M8070B Module View > Data Out > Parameters > Deemphasis > PCIe LTSSM Presets.

2. Click the Edit TxEQ Matrix icon.
The PCIe TxEQ Matrix Editor appears for the selected file. The PCIe TxEQ Matrix Editor title bar displays the module number and the factory file selected.
Exploring the TxEQ Matrix Editor User Interface

The **TxEQ Matrix Editor** user interface includes the following elements:

1. **Title Bar**
2. **Menu Bar**
3. **Matrix Setting pane**
4. **Matrix Editor Pane**
Setting up Generator

Title Bar
The title bar displays the application icon, title of the file, Options drop-down arrow, and the standard buttons to maximize or to close the window.

The Options drop-down arrow includes the following:
• Close - Closes the TxEQ Matrix Editor window.
• Dock - Docks the TxEQ Matrix Editor window with the other open tabs.

The title bar is shown in the following figure.

Menu Bar
The menu bar includes the following elements:

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
|          | New (CTRL + N) | Allows you to create a new matrix. For more information, refer to Creating a new matrix.  
|          |               | NOTE: This option is enabled only when you launch the TxEQ Matrix Editor through M8070B Menu Bar. |
|          | Open (CTRL + O) | Allows you to open an existing file to modify/edit.  
|          |               | On click of Open icon, the Open PCIe LTSSM deemphasis presets dialog box appears. For more information, refer to Opening an existing matrix.  
|          |               | NOTE: This option is enabled only when you launch the TxEQ Matrix Editor through M8070B Menu Bar. |
|          | Edit          | Allows you to make changes to an existing file.  
|          |               | For more information, refer to Editing an existing matrix. |
|          | Save (CTRL + S) | Allows you to save the file on your local system.  
|          |               | On click of Save icon, the Save PCIe LTSSM deemphasis presets dialog box appears.  
|          |               | NOTE: The Factory files cannot be saved using the Save option. Use Save as option to save any changes at different location. |
|          | Save as (F12) | Allows you to save a copy of opened matrix to a new location.  
|          |               | On click of Save as icon, the Save PCIe LTSSM deemphasis presets dialog box appears. |
Setting up Generator

Import (CTRL + I) Allows you to import any existing matrix file from any location to M8070B workspace to edit. On click of Import icon, the Select PCIe LTSSM de-emphasis presets To Import dialog box appears, which enables you to import the file. For more information, refer to Importing a matrix file.

NOTE: This option is enabled only when you launch the TxEQ Matrix Editor through M8070B Menu Bar.

Export (CTRL + E) Allows you to export the current matrix to a file to any location. On click of Export icon, the Open PCIe LTSSM de-emphasis presets dialog box appears, which enables you to export the file. For more information, refer to Exporting a matrix file.

Copy Allows you to copy any cell from the matrix editor. This option is enabled only when any cell/value is selected in matrix editor.

Paste Allows you to paste any valid value from clipboard to matrix value. This option is enabled only when there is any valid data to paste in the matrix editor.

Delete Allows you to delete any cell value from the matrix editor. This option is enabled only when any cell/value is selected in matrix editor.

Zoom-In/Zoom-Out Allows you to zoom-in and zoom-out the value of each cell of the matrix. By default, the matrix editor pane appears in Fit to Display mode.

Fit to Display Allows you to display the Matrix Editor pane in the current view without any scroll bars.

Show drop-down list Allows you to select an option from the Show drop-down list. The following options are available:
- Coefficient: Enables you to edit the cell values in the Matrix Editor pane.
- dB: Displays the matrix cell value in decibels. It displays the data in read-only mode, that is, the cell values cannot be edited in this mode.
Matrix Setting pane

The Matrix Setting pane enables you to change the settings of the matrix editor. This pane is accessible only when you launch the TxEQ Matrix Editor through the M8070B Menu Bar. For more information on launching, refer to Launching the TxEQ Matrix Editor through M8070B Menu Bar. The matrix settings pane enables you to set the Full Swing value and create the matrix. The acceptable range for Full Swing value is 24 - 63.
Matrix Editor Pane

The Matrix Editor pane enables you to edit any value of the opened matrix file. You can edit the value of the matrix cells when Show mode from the Matrix Setting is selected as Coefficient.

The Matrix Editor pane displays the following values in each cell:
- Pre-Cursor
- Main
- Post-Cursor

The Matrix Editor pane includes the following features:
- The horizontal pane displays the Post-Cursor value and the vertical pane displays the Pre-Cursor value.
- You can use the arrow keys, ENTER, TAB, or single click to navigate to the required matrix cell. The currently selected cell is highlighted by blue borders.
If you launch the TxEQ Matrix Editor through the M8070B Module View parameters window, you can press CTRL + ENTER or double-click the desired cell to apply the currently selected value to the respective channel. This feature is applicable only when you are in non-editing mode and data is displayed as coefficient.
Creating a new matrix

To create a new matrix, perform the following steps:

1. Go to **Menu Bar > Generator > TxEQ Matrix Editor**.

**NOTE** This option is available only when you launch the TxEQ Matrix Editor through M8070B Menu Bar.
5 Setting up Generator

The **PCIe TxEQ Matrix Editor - Untitled Matrix** window appears.

2 On the Tool Bar, click the New icon. By default, this option is displayed.

3 Under the Matrix Setting pane, do the following:
   a Enter the appropriate value in the Full Swing text box.
      
      You can use the Up/Down icons to increase or decrease the Full Swing value.
      
      The acceptable range for Full Swing value is 24 - 63.
   
   b Click Create.
The **PCIe TxEQ Matrix Editor** pane displays the matrix as per the value entered.

4. Click the **Save** icon to save the matrix.
The **Save PCIe LTSSM de-emphasis presets** dialog box appears.

![Save PCIe LTSSM de-emphasis presets dialog box](image)

5 On the **Save PCIe LTSSM de-emphasis presets** dialog box, do the following:

a. Select a folder where you want to save the file.

   By default, two folders; **Shared** and **Current** are available. Click **New Folder** to create a new folder.

b. Type an appropriate name for the file in the **File Name** text box.

c. Click **Save**.

The file is saved at the location. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.
If you start a new process (Open, Import, Export, or Close) without saving the current matrix, the **Save TxEQ Matrix** dialog box appears.

The following options are available:

- **Save Changes**: Saves the changes to the file. The **Save PCIe LTSSM de-emphasis presets** dialog box appears.
- **Continue without Save**: Continues with the new process without saving the current file to the system.
- **Cancel**: Cancels the new process and the user remains in the editor window.
Opening an existing matrix

To open an existing matrix, perform the following steps:

1. Launch the TxEQ Matrix Editor through M8070B Menu Bar.
   For more information, refer to Launching the TxEQ Matrix Editor through M8070B Menu Bar on page 295.

2. Click Open icon.
   The Open PCIe LTSSM de-emphasis presets dialog box appears.

3. On the Open PCIe LTSSM de-emphasis presets dialog box, select the appropriate file.

4. Click Open.
The TxEQ Matrix Editor displays the selected file. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.
5 Setting up Generator

Editing an existing matrix

To edit an existing file, perform one of the following:
- Editing an existing file (TxEQ Matrix Editor through M8070B Menu Bar)
- Editing an existing file (TxEQ Matrix Editor through M8070B Module View Parameters Window)

Editing an existing file (TxEQ Matrix Editor through M8070B Menu Bar)

When you launch the TxEQ Matrix Editor through M8070B menu bar, perform the following steps to edit an existing matrix.

1. Go to Menu Bar > Generator > TxEQ Matrix Editor.
   The PCIe TxEQ Matrix Editor - Untitled Matrix window appears.

2. Click Open icon to open an existing file for editing. Refer to Opening an existing matrix on page 310, for more information.
The TxEQ Matrix Editor displays the selected file.

3 On the PCIe TxEQ Matrix Editor, click the Edit icon.
3 Setting up Generator

The PCIe Matrix Editor enables you to edit the cell values.

4 After all the modifications are done, do one of the following:
   - Click **Save** icon to save the file.
   - Click **Save as** icon to save the copy of the file to a new location.

**NOTE**

The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.
When the **Save as** option is clicked, the **Save LTSSM de-emphasis presets** dialog box appears.

5 (Optional) On the **Save PCIe LTSSM de-emphasis presets** dialog box, do the following:

a Select a folder where you want to save the file.

   By default, two folders; Shared and Current are available. Click **New Folder** to create a new folder.

b Type an appropriate name for the file.

c Click **Save**.

The file is saved at the location. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.
Setting up Generator

Editing an existing file (TxEQ Matrix Editor through M8070B Module View Parameters Window)

When you launch the TxEQ Matrix Editor through M8070B module view parameters window, perform the following steps to edit an existing matrix.

1. Go to M8070B Module View > Data Out > Parameters > De-emphasis > PCIe LTSSM Presets.

2. Click the Edit TxEQ Matrix icon.

**NOTE**

When the Edit TxEQ Matrix icon is clicked, the Open, Import, Reset, and Edit TxEQ Matrix options are disabled under the PCIe LTSSM Presets parameter.

When the Matrix Editor window is closed, these options are enabled again.
The TxEQ Matrix Editor appears for the selected file. The New, Open, Save, Save as, Import, Copy, Paste, and Delete options are disabled.

3 On the PCIe TxEQ Matrix Editor, click Edit icon.

NOTE

You can select another channel through the M8070B main window, even when the TxEQ Matrix Editor is already opened for a particular channel. When selected, all the buttons are enabled for this channel.

When you click the Edit TxEQ Matrix Editor icon for the new channel, the TxEQ Matrix Editor displays the selected file, and the PCIe TxEQ Matrix Editor title bar displays the name of the selected file.
The PCIe Matrix Editor enables you to edit the cell values.

The Save, Save as, Copy, Paste, and Delete icons are enabled in Edit mode. The Save option is enabled when you modify any of the cell value.

4 After all the modifications are done, do one of the following:
   - Click **Save** icon to save the file.
   - Click **Save as** icon to save the copy of the file to a new location.

**NOTE**

The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.
When the **Save as** option is clicked, the **Save LTSSM de-emphasis presets** dialog box appears.

5. (Optional) On the **Save PCIe LTSSM de-emphasis presets** dialog box, do the following:
   a. Select a folder where you want to save the file.
      By default, two folders; Shared and Current are available. Click **New Folder** to create a new folder.
   b. Type an appropriate name for the file.
   c. Click **Save**.

The file is saved at the location.
5 Setting up Generator

Importing a matrix file

To import an existing matrix file from any location to M8070B workspace, perform the following steps:

1. Launch the TxEQ Matrix Editor through M8070B Menu Bar.
   For more information, refer to Launching the TxEQ Matrix Editor through M8070B Menu Bar.

2. Click **Import** icon.
   The Select PCIe LTSSM de-emphasis presets To Import dialog box appears.

3. Browse the required matrix file, and then click **Open**.

4. In the Save PCIe LTSSM de-emphasis presets dialog box, type an appropriate name in the **File Name** text box.
5 Click **Import**.
The selected file is imported successfully. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.

6 *(Optional)* Click **Open** icon to check the imported file.

The imported file is opened in Matrix Editor.
Exporting a matrix file

To export the current matrix to a file to any location, perform the following steps:

1. Launch the TxEQ Matrix Editor. For more information, refer to "Launching the TxEQ Matrix Editor".

2. Click the Export icon.
   The Open PCIe LTSSM de-emphasis presets dialog box appears.

3. Select a file, and then click Open.
The Export PCIe de-emphasis presets File dialog box appears.

4 Type the name of the file in the File name text box, and then click Save.
The File Exported at [Location name] message appears.

5 Click OK.
Adjustable Intersymbol Interference

The M8070B system software provides integrated and adjustable Intersymbol Interference (ISI) capability to test next-generation high-speed digital designs.

The adjustable and programmable ISI function allows emulating channel loss for characterizing and compliance testing of high-speed digital receivers. This function is integrated in each pattern generator channel of the M8020A/M8030A which streamlines test setup by eliminating the need for external cabling and switching of external ISI traces.

As data rates continuously increase, channel loss between transmitter and receiver becomes more important. Channel loss is caused by printed circuit board traces, connectors, and cables in the signal path; resulting in ISI which depends on the channel material and dimensions, the data rate, and bit pattern. All high-speed digital receivers are specified to tolerate a certain amount of total jitter, which typically includes some ISI caused by channel loss. During receiver characterization and compliance test, this loss needs to be emulated.

The built-in ISI functionality is programmable for each pattern generator channel. It simplifies receiver test automation for data rates up to 16 Gb/s.

The new adjustable ISI option offers the following advantages:

- Streamlines receiver test setup by providing the highest level of integration.
- Provides accurate and repeatable results for receiver characterization and compliance test by supporting a wide range of loss up to 25 dB and 16 GHz with linear loss curves and fine step resolution.
- Fits into the fully scalable and upgradeable receiver test solution with an upgrade option.

Using System View for ISI Configuration

You can use the System View to configure the ISI parameters for a selected 'Data Out' location. When you select ISI in the Jitter block of the System View, the corresponding parameters are loaded on the Parameters window. You can create your own preset or manipulate frequency and insertion loss for the selected preset.
However, the System View does not provide flexibility to graphically manipulate the ISI parameters. This can be achieved using the Adjustable ISI window.

How to Launch Adjustable ISI Window:

To launch the Adjustable ISI window

- Go to the Menu Bar > Generator and then select Adjustable ISI.

The Adjustable ISI window will appear as shown in the following figure:
It includes the following elements:
- Toolbar
- Adjustable ISI Graph
- ISI Parameters

**Toolbar**

The toolbar provides the following convenient adjustable ISI functions:

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Open SnP File</td>
<td>Click this button to open an s-parameters file (S2P). Currently, the M8070B GUI supports two port (S2P) and four port (S4P) s-parameters files. The s-parameters (also known as scattered parameters) are displayed when the scattered pattern file is loaded. S-parameters are complex matrix that show insertion loss at certain frequency. The two-port device displays four data points while the four-port device displays sixteen data points.</td>
</tr>
<tr>
<td></td>
<td>Channel Selection</td>
<td>Use this drop-down list for channel section for which the graph is plotted for the corresponding values.</td>
</tr>
</tbody>
</table>
Adjustable ISI Graph

The following figure illustrates an ISI graph for 4-port system:

The ISI graph shows the insertion loss for a 2-port or 4-port system. The values on the graph represents insertion loss with respect to frequency. You can select the data points according to which you want to generate the loss and then manipulate points graphically (mouse drag) or by parameter window to draw the data point graph. Please note that if you manipulate the points of the linear graph to the values which are not in the defined limits of Slope and Offset, the pointer will change to ⏪ icon. In this case, the linear graph will switch to last set values. However, if you manipulate the points of the linear graph to the values which are not in the defined limits of Slope and Offset, the pointer will change to ⏪ icon. In this case, a message will appear at the bottom of the graph along with the undo option to revert the graph changes.

ISI Parameters

The ISI parameters are summarized in the following list:

- **State** - Enables/disables the ISI state.
- **Preset** - Allows you to select preset for specific applications representing a typical loss characteristic.
• **Mode** - Controls the ISI as one point or two points. For each point you can specify frequency and insertion loss at that frequency. The calculated values are displayed in the **Parameters** window.
  - **One Point**: In this mode, one point of the linear graph is fixed while the another point can be moved graphically to manipulate insertion loss/frequency values.
  - **Two Points**: In this mode, both points of the linear graph can be moved graphically to manipulate insertion loss/frequency values.
• **Slope** - Shows the calculated slope value (Insertion Loss/frequency, dB/GHz).
• **Insertion Loss Offset** - Shows the Insertion Loss Offset (at frequency=0 Hz).

**Intersymbol Interference (ISI) Setup**

The following steps describe the procedure for ISI setup:

1. Connect the DUT in loopback mode. For connection details, refer to M8020A and M8030A Getting Started Guide.
2. From the M8070B software, launch **Adjustable ISI** window.
3. Select **M1.DataOut1** channel from drop-down list.
4. From the **Parameters** window, select the **Preset** from the provided list. It will show the linear graph.
5. Select the mode as **Two Points**.
6. Manipulate insertion loss/frequency values either graphically or by **Parameters** window.
7. Alternatively, you can also open a S2P or S4P file and graphically manipulate loss and frequency parameters according to data points.
8. Click the toggle button to enable the ISI state.
6 Setting up Analyzer

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Overview

The M8020A/M8030A/M8040A Analyzer examines an incoming bit stream, compares it to the expected pattern, and locates any inconsistencies. The Analyzer requires the following settings to work correctly:

- The expected pattern
  The Analyzer needs to "know" which data to expect so that it can detect bit errors. No expected patterns are required in BRM mode.
- Correct clock frequency
  Required to recognize the bit rate in the data stream.
- Appropriate sampling point
  The sampling point defines where the Analyzer tries to differentiate between 0s and 1s in the data stream. This is necessary so that the Analyzer recognizes the data bits correctly.
- Synchronization to the incoming pattern
  The expected pattern must be synchronized to the incoming pattern so that the Analyzer can find any discrepancies.

The Analyzer provides the following functions to enable you to perform tests:

- Automatic pattern synchronization
  The Analyzer shifts the incoming data stream bitwise to match it to the expected data pattern. A correct BER can only be measured with matching patterns.
- Error accumulation
  You can specify whether a test runs for a specified time or until a specific number of errors has occurred. This lets you carry out longer tests while logging the results to a file.
- BER location mode
  You can specify whether all errors are counted or only the errors that occurred on a particular bit position or range of positions.
- Trigger output for external measurement instruments
  This allows you to connect other devices for further error analysis.
- Data format
  The M8040A (M8046A) analyzer has an enhanced capability over M8020A analyzer to analyze PAM4 data in addition to NRZ.
M8020A/M8030A/M8040A Analyzer Ports

The M8020A/M8030A/M8040A analyzer’s ports are used for running tests and for connecting external equipment.

The following figure shows the J-BERT M8041A analyzer’s ports.

The M8041A analyzer’s ports include the following:

- Data In and Data In
  This port is connected to the data signal and the inverted data signal.

The following figure shows the M8040A analyzer’s (M8046A) ports.

The M8046A analyzer’s ports include the following:

- Data In and Data In
  This port is connected to the data signal and the inverted data signal.
- Clk In
  This is a clock input port to sample the incoming data. Supports full/half and quarter-rate clock. Single ended.
- Ctrl In A
  This port can be used as sequence trigger or pattern capture event.
- Ctrl Out A
  This port outputs a pulse in case of an error. It generates a pulse or static high/low if used from sequencer.
Data In Port Termination

To ensure a valid setup and to protect the devices from damage, proper termination must be specified for both Data In connections. You can specify the termination by entering the termination voltage in the respective field.

**CAUTION**

Selecting the wrong termination may damage your device.

---

Why Can Wrong Terminations Damage Your Device?

Choosing wrong terminations may cause your device to output voltage levels that are not as expected. It may also cause excessive current or current flow in the wrong direction, which can damage your device.

If you adjust the termination voltage, and try to enter value(s) which are outside of the currently allowed window, the Auto Correction Confirmation message box will pop up with respective apply and discard options as shown in the following figure:

![Auto Correct Confirmation](image)
Setting Up Termination

To select the termination for the Analyzer:

**NOTE**
You must know the termination voltage of the data signal that your DUT sends to the Analyzer.

1. Go to the **Menu Bar** > **Analyzer** and then select **Data In**.
2. Select **Comparator** functional block from the **Parameters** window.
3. In the **Termination Voltage** field, enter the termination voltage that is appropriate for the incoming data signal.

**CAUTION**
Selecting the wrong termination may damage your device.

4. In the **Polarity** field, select **Inverted** if your device inverts data.

You can now physically connect the DUT to the Analyzer.

**Compare Mode**

The selection in this list defines how the signals arriving at the **Data In** and **Data In** connectors are interpreted. The following options are available:

- **Differential**
  If differential mode is selected, both input ports need to receive a signal. The actual data signal is measured as the voltage difference between the two incoming signals.
- **SE-Normal (Single Ended - Normal)**
  In normal mode, only the **Data In** port receives the data signal, the **Data In** port is inactive.
- **SE-Complement (Single Ended - Complement)**
  In complement mode, only the **Data In** port receives the data signal, the **Data In** port is inactive.
- **Single-Ended**
  In the Single-Ended mode, the data stream is provided at either Normal input or Complement input. The other input is either left open or terminated with 50 Ohm.
The availability of the particular compare mode selection depends on the currently used hardware.

The following drawing is an example how the instrument internal circuitry looks like for different settings.

This figure is only true for M8041A and M8051A modules with serial numbers < DE55300500.

VT = Termination Voltage
VC = Common Mode Voltage

This figure shows what the analyzer represents as termination scheme to the DUT. The DUT would be connected to the connectors shown on the left part of the respective schemes above.

For the balanced settings the internal termination voltage of the analyzer is set to equal the Common Mode Voltage, which must be given by the user in the GUI.
The following figure shows a slightly modified figure for the analyzer part:
This figure is true for M8041A and M8051A modules with serial numbers >= DE55300500.

VT = Termination Voltage

This figure shows what the analyzer represents as termination scheme to the DUT. The DUT would be connected to the connectors shown on the left part of the respective schemes above.
Data Inverted

To activate data inverted function, select the Polarity as Inverted in the Comparator functional block of the Analyzer. This function is required if your device inverts data.

Threshold

Enter a Threshold value for applications that do not provide a continuous data stream at the input (for example, any application using bursts), because the averaged threshold voltage will drift from the correct level when there is no input.

PAM4 Decision Threshold

It is only available for PAM4 line coding. It controls the decision threshold of the PAM4 decoder within the data input’s input window. The setting of the PAM4 decision thresholds always refers to the actual input voltage range.

The following 3 decision thresholds are applied:

<table>
<thead>
<tr>
<th>Threshold</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower</td>
<td>Decides between symbol 0 and symbol 1.</td>
</tr>
<tr>
<td>Middle</td>
<td>Decides between symbol 1 and symbol 2.</td>
</tr>
<tr>
<td>Upper</td>
<td>Decides between symbol 2 and symbol 3.</td>
</tr>
</tbody>
</table>
## Termination Voltage

In this field, enter the termination voltage that is appropriate for the incoming data signal. This selection should be made before the device is connected to the analyzer.

**CAUTION**

Selecting the wrong termination may damage your device.

The **Data In** port is connected to a 50 \( \Omega \) load impedance (or termination) within the **Analyzer**. Data termination refers to the voltage level at the end of this load. The logic output from a device requires any connected equipment, including the **Analyzer**, to have a specific termination voltage.

## Input Range

Before you can synchronize the **Analyzer** to the incoming data stream, you need to define the voltage range within which the eye is located.

Both the high and low level of the data signal must be within this range to find the eye.

**NOTE**

The input voltage range for M8020A and M8040A is 2V and 500 mV, respectively. When you modify either the high or low voltage, the other voltage is automatically adjusted.
Squelch Threshold

The Squelch Threshold feature allows you to adjust the squelch threshold values in link training applications (e.g. USB link training).

This feature is only available with M8020A modules (M8041A and M8051A).

It has the following parameters:

- **Squelch Threshold Mode** - Use this parameter to select either Auto or Manual mode. In the Auto mode, the instrument works with factory calibrated values. In the Manual mode, user is allowed to adjust the current squelch threshold value.

  The following figure shows the available parameters in the Manual mode:

  ![Squelch Threshold Panel](image)

  - **Squelch Threshold Value** - Use this parameter to set the squelch threshold value in range from 0 ... 255.
  - **Preset Button** - Use this button to set the default squelch threshold value.
Input Sensitivity

The Sensitivity parameter enables you to set the error detector input sensitivity to normal or high.

**NOTE**

This feature is only available with M8020A modules (M8041A and M8051A).

1. Go to **Menu Bar > Analyzer** and then select **Data In**.
2. Select **Comparator** functional block from the **Parameters** window.
3. From the **Sensitivity** drop-down list, select an option.
   The following options are available:
   - Normal
   - High

<table>
<thead>
<tr>
<th>Input sensitivity</th>
<th>50 mV typical @ normal sensitivity mode†</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>40 mV typical @ high sensitivity mode‡</td>
</tr>
</tbody>
</table>

* Measured with PRBS $2^{31} - 1$ at 16 Gb/s, AC coupling mode, BER of 10-12, CTLE disabled.

† Eye height measured at input of reference cable M8041A-801 with DCA-X module 86117A. Applies for single ended and differential input signals.
Clock Setup

To measure the Bit Error Rate with the Analyzer, the bit rate of the data stream must be known. Depending on the options the instrument is delivered with, you could use either an external clock source for the Analyzer (for example, the clock from the generator), or extract the clock signal from the incoming data (CDR mode).

CDR mode does not work for all kinds of data patterns. For example, if the device under test sends only blocks of ones and zeros, there are no transitions in the data stream and the M8020A/M8030A cannot recover the clock.

Also, if you are testing bursts, there are some special considerations for setting up CDR.

How does Clock Data Recovery Work?

In CDR mode, the CDR has to recover the clock from the incoming data. To do this, the hardware has to decide whether the voltage at the input connector is a logical '1' or '0' and then recover the clock from the detected transitions.

Clock Data Recovery (CDR) is a special kind of Phase Locked Loop (PLL), which recovers clock signal of a data stream. It is a regulatory loop, which synchronizes the local oscillator with an external reference, in this case the incoming data stream.

Phase Locked Loop

A PLL has three parts: a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector has two inputs, and one output, which is proportional to the phase difference of the inputs. The loop filter is a low pass filter which attenuates the higher frequencies from the output of the phase detector. The VCO is an adjustable oscillator which changes the output frequency depending on its input voltage. The diagram below shows a simple PLL.
One of the most important characteristics of a PLL is its loop transfer function. The loop bandwidth is defined as the integrated magnitude of the PLL’s frequency transfer function over the entire frequency spectrum. The loop bandwidth describes how the regulatory loop tracks the VCO to a sine wave FM modulated input signal. Above the bandwidth the loop cannot track such a modulation completely, and thus, the response to the modulation is attenuated.

The other loop parameter is peaking. This describes how much a modulation is exaggerated (mostly close to the loop bandwidth).

**Transition Density**

The transition density is defined by the number of transitions in the incoming data divided by the total number of bits transmitted. In this field enter the transition density in (%).

This parameter affects the loop bandwidth, and thus must be entered correctly. Some standards specify the loop bandwidth for a given transition density. In such a case enter the value given in the specification, so that the CDR behaves according to the standard. If a standard from the preset list is selected, this field is also preset.

**Loop Bandwidth**

This is the range of the CDR loop bandwidth. In this field the user should enter the loop bandwidth value; the range is within 313 kHz to 20 MHz.

When the M8020A/M8030A Analyzer is used to characterize a data stream instead of a receiver, the loop parameters should be set according to the used standard.

If the CDR is used to recover the bit stream from a receiver to be characterized due to a lack of a clock output, choose the loop bandwidth significantly higher than the receiver’s bandwidth. To characterize a DUT’s
CDR it is the best practice to use its recovered clock output instead of the M8020A/M8030A’s built in CDR. Choose a low loop bandwidth to measure the jitter on an incoming data stream as the CDR will track the incoming jitter up to the loop bandwidth and thus make it invisible to the Analyzer.

**CDR Spread Spectrum Clocking**

This control is used to adapt the CDR to an input bit stream with SSC. Enabling SSC state widens the loss of lock detection window, and sets the peaking to optimum SSC performance. Enter the **Expected Deviation** and the type of deviation (Up-Spread, Down-Spread or Center-Spread) to set the locking window to an optimum.

SSC is mostly used **Down-Spread** which means, the clock signal is modulated to a lower frequency and back. Thus the average frequency is lowered by half of the maximum deviation. The CDR is adapted to that value. Enter the maximum deviation as specified in the standard.

**CDR Setup in M8020A/M8030A**

The M8020A/M8030A has an internal CDR. Follow the given steps to perform a CDR Setup:

1. Go to the **Menu Bar > Analyzer** and then select **Data In**.
2. Select **CDR** functional block from the **Parameters** window. The following parameters will appear:

![CDR Parameters Window]

3. Click **CDR State** switch to turn on the CDR state.
4. Specify the CDR parameters setting. For details on CDR parameters, refer to **M8020A/M8030A CDR Parameters** on page 343.
The M8020A/M8030A has the following parameters:

- **Control**: You can specify whether the CDR is controlled by the pattern sequence or if it is manually enabled or disabled.
- **CDR State**: It enables or disables the CDR state.
- **Transition Density**: It affects the loop parameters, and it must be either entered, or measured. Some standards define a loop bandwidth for a specific transition density.
- **Loop Order**: The data stream contains multiple frequencies, and the CDR needs to know the expected data rate. You can choose between 2 types of CDR; 1st order and 2nd order.
- **Loop Bandwidth**: It is the input parameter to set the characteristics of the loop.
- **Peaking**: Additionally, you can set the value for peaking in the provided field. It defines the second order CDR characteristics by defining a peaking value which is valid for jitter transfer function. The peaking parameter is only available for the second Loop Order.

### CDR Setup for M8040A

The M8040A system supports internal as well as external CDR.

#### Internal CDR Setup

The M8040A system has an internal CDR. Follow the given steps to perform a CDR Setup:

1. Go to the Menu Bar > Analyzer and then select Data In.
2. From the Parameters window, select the clock source as “CDR”. The following parameters will appear:
3. Click **CDR State** switch to turn on the CDR state.

4. Specify the CDR parameters setting.
   - **Control**: You can specify whether the CDR is controlled by the pattern sequence or if it is manually enabled or disabled.
   - **Output State**: It enables or disables recovered clock signals at the Rec Clk Out.
   - **Auto Re-Lock**: It enables or disables the automatic clock recovery locking.
   - **Transition Density**: It affects the loop parameters, and it must be either entered, or measured. Some standards define a loop bandwidth for a specific transition density.
   - **Loop Order**: The data stream contains multiple frequencies, and the CDR needs to know the expected data rate. You can choose between 2 types of CDR; 1st order and 2nd order.
   - **Loop Bandwidth**: It is the input parameter to set the characteristics of the loop.
   - **Loop Selection**: It specifies type 2 loop transition frequency and thereby the JTF peaking. The choices are Loop1, Loop2, Loop3 and Loop4.
- **Peaking**: Additionally, you can set the value for peaking in the provided field. It defines the second order CDR characteristics by defining a peaking value which is valid for jitter transfer function. The peaking parameter is only available for the second Loop Order.

**External CDR Setup**

The N1076A/77A can be assigned to an M8046A error detector to be used as an external clock recovery. In this case, M8046A will ensure that certain critical parameters are automatically kept in sync between M8046A and N1076A/77A. To use the N1076A/77A from within M8070B, the FlexDCA N1000-Series System Software has to be started and fully running before starting M8070B. Once all these instruments are connected, start the M8070B software. For details on connections and how to access N1076A/77A from within M8070B, refer to **M8070B Advance Measurement Package User Guide**.

Follow the given steps to perform a CDR Setup:

1. Go to the **Menu Bar > Analyzer** and then select **Data In**.
2. Select **Clock** functional block from the **Parameters** window. The following parameters will appear:

![Clock parameters](image)

3. Select 'Ext. Clock Recovery' as Clock Source of M8046A.
4. Choose one of the available external clock recoveries under "External Clock Recovery".

For further details, refer to **M8070B Advance Measurement Package User Guide**.
Sampling Point Setup

This section provides basic information on the sampling point setup.

How Does the Sampling Point Setup Work?

The sampling point of a data signal is defined by two values: a point in time and a voltage level. Each bit of the data signal is sampled at this point in time and in reference to this voltage level. The point in time (in reference to the clock signal) is referred to as the data input delay, and the voltage level is referred to as the threshold.

The location of the sampling point is the decision factor as to whether the incoming bits are identified as logic 0's or 1's. To measure the accurate bit error ratio at the input port, false readings of logic 0's or 1's must be avoided. Therefore, the sampling point must be set to the optimum location within the data eye.

The functions within the Sampling Point Setup window allow you to:

- Prepare the Analyzer for the incoming data signal regarding the connector termination.
- Adjust the location of the sampling point.

For details on Sampling Point Setup window, see Sampling Point Setup Window on page 349.

Auto Alignment

Use this option to automatically set the optimum sampling point.

To perform the Auto Alignment:

1. Go to the Menu Bar > Analyzer and then select Data In.
2. Select Analyzer function block from the Parameters window.
3. Specify Alignment BER Threshold form the provided list.
4. Click Execute button for the align sample delay and decision threshold voltage to the received data.
5 Alternatively, you can click on Alignment BER Threshold button present on the Status Indicator to start BER threshold auto alignment.

This routine will not stop if the optimum sampling point cannot be found. If no optimum sampling point is found after a reasonable time, you can click Abort.

The following settings may affect the result of the auto align function:
- Polarity (Data Inverted)
- Threshold (BER Threshold)

**NOTE**

When the line coding “PAM4” is selected for the loopback mode, it is recommended to adjust the pattern generator data output de-emphasis for the post cursor for error free operation (e.g. +0.05 at 25 Gbaud).

---

**Threshold Center Alignment**

To perform the Threshold Center Alignment:

1. Go to the Menu Bar > Analyzer and then select Data In.
2. Select Comparator function block from the Parameters window.
3. Specify the Threshold and then click Execute button for the threshold center alignment.

The threshold center alignment starts an auto-search function that sets the threshold to the optimum point of the incoming data eye on the vertical voltage axis without changing the data input delay. This function can be used for determining the optimum threshold for asymmetric data eyes, or for patterns with an unequal mark density.

**NOTE**

This function uses the alignment BER Threshold to determine the top and bottom eye edges.
Delay Center Alignment

To perform the Delay Center Alignment:
1. Go to the Menu Bar > Analyzer and then select Data In.
2. Select Input Timings function block from the Parameters window.
3. Specify the Delay and then click the Execute button to align the sample delay to the received data.

This button starts an auto-search function that aligns the data signal with the clock signal so that the Analyzer samples at the optimum point of the data eye in the time axis. This automatically compensates for delays in the clock/data paths, preventing unnecessary errors. The decision threshold is not changed.

**NOTE**
Ensure that the received clock frequency is stable before using Data Center.

**NOTE**
The clock/data alignment process time is pattern dependent, and with some large user patterns the alignment can take several minutes. If you encounter such a long time with a user pattern, it may be possible to first perform clock/data alignment on a pure PRBS pattern. This generally does not affect alignment accuracy, and can minimize measurement time.

This tip does not apply in cases of severe pattern dependent jitter or with devices that do not work with PRBS patterns.

**NOTE**
This function uses the alignment BER threshold to determine the left and right eye edges.
Canceling Auto Align

Click this button to cancel the Auto Align, Threshold Center, or Data Center functions while they are in progress. The following parameters will be returned to their previous value or status:

- Auto Align Canceled
  - Data Delay and Threshold values returned to previous.
- Threshold Center Canceled
  - Threshold value returned to previous.
- Data Center Canceled
  - Data Delay value returned to previous.

Alignment BER Threshold

In this list, select an alignment BER threshold that is appropriate for your application.

The alignment BER threshold is the pre-defined threshold used by the Auto Align, Threshold Center, and Data Center functions to define the edges of the data input eye in the time and voltage axes. You may wish to change the threshold for the following reasons:

- Choosing smaller alignment BER thresholds will cause the auto-search functions to set more accurate sampling points. However, if the BER threshold is set lower than the residual BER of the measurement, the auto-search functions will fail. 1E-9 is the smallest BER threshold available.

Sampling Point Setup Window

The Sampling Point Setup window allows you view and then manually adjust the location of the sampling point.

It can be accessed though the Menu Bar. Go to Menu Bar and then click Analyzer > Sampling Point Setup. However, if you are in the Setup View window, you can click on the Manual Alignment... button to open the Sampling Point Setup window.

The following figure shows the sampling point setup window for M8020A system (M8041A and M8051A):
The vertical axis represents the threshold voltage value and the horizontal axis represents delay which can be used to manually adjusted the location of sampling point.

For M8040A system (M8045A and M8046A), the **Sampling Point Setup** window display histograms which represents number of times a signal has achieved a particular threshold. For PAM4 line coding, the **Sampling Point Setup** window shows three vertical voltage axis which represents Upper, Middle and Lower threshold value which can be used to manually adjusted the location of sampling point. For NRZ line coding, the **Sampling Point Setup** window shows two vertical voltage axis which represents Upper and Lower threshold value which can be used to manually adjusted the location of sampling point.

The following figure shows the **Sampling Point Setup** window displaying histograms and vertical voltage axis for PAM4 line coding:
The GUI elements provided in the **Sampling Point Setup** window user interface depends on the type of selected analyzer channel. The following table describes the elements provided by the **Sampling Point Setup** window:

<table>
<thead>
<tr>
<th>GUI Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Select Channel</td>
<td>Use this drop-down list to specify the Analyzer's channel on which sampling should be done.</td>
</tr>
<tr>
<td></td>
<td>Optimize Input Range</td>
<td>Click this button to adjust the input voltage window to match the received signal at the Data In connectors. This button is available when the sampling is done using the M8046A analyzer module.</td>
</tr>
<tr>
<td></td>
<td>Optimize Equalizer Coefficients</td>
<td>Click this button to optimize the equalizer settings, using the current coefficient setting as a starting point. This button is available when the sampling is done using the M8046A analyzer module.</td>
</tr>
<tr>
<td></td>
<td>Auto Align</td>
<td>Click this button to automatically set the optimum sampling point. This routine will not stop if the optimum sampling point is not found.</td>
</tr>
</tbody>
</table>
### Setting up Analyzer

<table>
<thead>
<tr>
<th>GUI Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="align_threshold_button" /></td>
<td>Align Threshold</td>
<td>Click this button to start an auto-search function that sets the threshold to the optimum point of the incoming data eye on the vertical voltage axis without changing the data input delay.</td>
</tr>
<tr>
<td><img src="image" alt="align_data_button" /></td>
<td>Align Data</td>
<td>Click this button to start an auto-search function that aligns the data signal with the clock signal so that the error detector samples at the optimum point of the data eye in the time axis. This automatically compensates for delays in the clock/data paths, preventing unnecessary errors.</td>
</tr>
<tr>
<td><img src="image" alt="reset_sampling_point_button" /></td>
<td>Reset Sampling Point</td>
<td>Click this button to return the Threshold and Data Delay to the values measured during the last auto alignment.</td>
</tr>
<tr>
<td><img src="image" alt="pattern_sync_button" /></td>
<td>Pattern Sync</td>
<td>Click this button to manually initiate the pattern synchronization. This is recommended whenever you did changes to the pattern setup, the voltage levels or the hardware connections (for example, altered cable lengths). Pattern synchronization is not required if it is selected as “Automatic” in the Analyzer functional block.</td>
</tr>
<tr>
<td><img src="image" alt="automatic_re_sync_manual_re_sync" /></td>
<td>Automatic Re-Sync / Manual Re-Sync</td>
<td>Use this drop-down list to choose whether you want and automatic or manual synchronization.</td>
</tr>
<tr>
<td><img src="image" alt="auto_refresh_button" /></td>
<td>Auto Refresh</td>
<td>Use this toggle button to automatically refresh the histogram. This option is available when the sampling is done using the M8046A analyzer module.</td>
</tr>
<tr>
<td><img src="image" alt="accumulate_button" /></td>
<td>Accumulate</td>
<td>Use this toggle button to accumulate histogram for the specified time (in seconds). Use the up and down arrows to specify the time. This option is available when the sampling is done using the M8046A analyzer module.</td>
</tr>
<tr>
<td><img src="image" alt="scale_button" /></td>
<td>Scale</td>
<td>Use this drop-down list to view measured histogram of the received signal on various scales (linear, logarithmic or both). This option is available when the sampling is done using the M8046A analyzer module.</td>
</tr>
</tbody>
</table>
How to Set the Sampling Point Automatically

In most cases, you will set up the sampling point automatically. Even if you wish to make some manual adjustments, it is recommended to start with automatically aligning the sampling point. For automatically aligning, press the Auto Align button. It will automatically set the optimum sampling point as shown in the following figure:
For the PAM4 line coding in M8046A analyzer, it will automatically set the optimum sampling point as shown in the following figure:

How to Adjust the Sampling Point Manually

For manual adjustments, select the vertical voltage axis and move the sampling point vertically towards other location at the selected delay. The same can also be done by changing the Threshold value in the Parameter window. The Sample Point on the sampling diagram moves vertically as you change the value.

In case of PAM4 line coding in M8046A analyzer, there are three vertical voltage axis which represents Upper, Middle and Lower threshold value. You can move the sampling point vertically towards the other location at the selected delay.

The same can also be done by changing the Upper, Middle and Lower threshold value in the Parameter window.

Similarly, select the horizontal axis and move the sampling point horizontally towards the other location at the selected voltage. The same can also be done by changing the Delay value in the Parameter window. The Sample Point in the sampling diagram moves horizontally as you change the value.
How to View Measured Histogram on Different Scales

The Sampling Point Setup allows to view the measured histogram of the received signal on different scales.

- **Linear Scale**
  
  Draws the histogram using a linear scale for the hit count.

- **Logarithmic Scale**
  
  Draws the histogram using a logarithmic scale for the hit count.
• Both Scales
  Draws the histogram twice, using both scales (linear and logarithmic).
Equalization

Equalization is used to correct for the problems caused by the transmission channel. Equalization techniques provide a way to discern the original signal (the signal coming out of the transmitter) given a distorted signal at the receiver.

In other words, equalization corrects for the high-frequency component voltage levels and, in the process, corrects the trajectories of these components in the corresponding eye diagram (that is, opens up the eye).

The M8070B software provides integrated and adjustable equalization capabilities to compensate the loss characteristic in an incoming signal.

Equalization in M8041A/M8051A Data In

The M8041A/M8051A Data In provides pre-defined equalization presets on incoming signals for specific applications e.g. PCIe, USB. The calibration of the equalization is only valid for these specific applications.

Follow the given steps to perform equalization in the M8041A/M8051A Data In:

1. Go to Menu Bar > Analyzer and then select Data In.
2. Select Input Timing functional block from the Parameters window.
3. Select the Equalization presets from the provided drop-down list.

The M8041A-0A3 or M8051A-0A3 license is required to enable the equalization feature in M8041A Data In or M8051A Data In, respectively.
Equalization in M8062A Data In

The M8062A Data In provides pre-defined equalization presets on incoming signals for the data rates above 20 Gb/s.

**NOTE**

The Equalization option in the M8062A user interface will be enabled for the data rates above 20 Gb/s.

Follow the given steps to perform equalization in the M8062A Data In:

1. Go to Menu Bar > Analyzer and then select Data In.
2. Select Input Timing functional block from the Parameters window.
3. Select the Equalization preset from the provided drop-down list. The available equalization presets are Low, Medium or High.

**NOTE**

The M8062A-0A3 license is required to enable the equalization feature in M8062A Data In.
Equalization in M8046A Data In

The M8046A analyzer allows you to either enter the equalizer coefficients manually or use the preset levels. The direct input of the equalizer coefficients allows fine tuning the equalizer to a degree which is not possible with the preset levels.

The following modes are available:

• Preset defined by the Equalizer Level
  This includes automatic compensation of the standard cables for either the error detector alone, or the error detector plus the additional required data cables and pick-offs in case of external clock recovery usage.

• Manual entry with cable compensation
  This mode allows the user to configure the filter coefficients manually, while still having the same automatic standard cable compensation in place that is being done in the Preset mode.

• Manual entry without cable compensation
  This mode allows the user to configure the filter coefficients manually. No cable compensation is being done. Therefore this mode can be used if the measurement setup is not using the standard cables. E.g. when using shorter cables, where the automatic cable compensation will result in overcompensating the cables even on the lowest equalization setting.

User Parameters

• Selection of equalization-mode
  • Equalizer Presets with cable compensation
    The equalizer gain is controlled as Equalizer Level, and the losses of the standard cabling is automatically included in the equalizer setting.
  • Manual coefficient entry with cable compensation
    The coefficients of the Feed Forward Equalizer can be entered manually. Additionally the losses of the standard cabling is automatically included in the equalizer setting.
  • Manual coefficient entry
    The coefficients of the Feed Forward Equalizer can be entered manually. No cable losses are automatically compensated. Use this mode when using non-standard cabling.
Setting up Analyzer

- FIR filter coefficients
  There are 16 filter coefficients, numbered from 0 to 15. Coefficient 2 is the main-cursor and cannot be changed.
  The available value range depends on the coefficient and is defined as follows:
  - Coefficient 0: -0.25 .. + 0.25
  - Coefficient 1: -0.5 .. + 0.5
  - Coefficient 2: 1.0
  - Coefficient 3: -0.5 .. +0.5
  - Coefficient 4: -0.25 .. + 0.25
  - Coefficient 5: -0.125 .. +0.125
  - Coefficient 6 to 15: -0.0625 .. +0.0625
  Additionally the sum of all 16 coefficients may not be 0.

User Interface for Equalization in M8046A

Preset Mode
In this mode, the equalizer gain is controlled by the Equalizer Level.
This mode can be used for quick pre-configuration of the filter coefficients before starting with manual fine tuning of individual filter coefficients.
The M8046A provides integrated and adjustable equalization capabilities on the data input to compensate for the loss characteristic of the back channel. Equalization can be adjusted from no equalization (0) to maximum equalization (120) in equidistant steps. This feature is available for NRZ and PAM4 signals and requires M8070B software 4.0 or higher.

The equalization is always automatically compensating the required reference cables (M8046A-802 or N4910A). This applies also when an external clock recovery N1076A/N1076B/N1077A/N1078A is used for the recommended pick-off and reference cables. It is mandatory to use the specified cables and pickoffs. Keysight recommends to use the reference cables (refer to M8040A data sheet) because other cables will lead to over/under-compensation of the input signal.
After changing the equalization level, it is required to re-adjust the threshold voltages again, or use the auto-alignment to re-optimize the sample point setting.

The M8046A Error Detector provides 120 pre-defined equalization levels for NRZ signals and 55 equalization levels for PAM4 signals. These equalization levels can be adjusted on the data input to compensate for the loss characteristic of the back channel. Specifications on these equalization levels can also be found in M8040A data sheet.

Manual Mode with Cable Compensation

This mode allows configuring the filter coefficients directly. It still adds the standard cable compensation that is done in Preset mode.

Note, that the coefficients will be set to default when switching from Preset mode to Manual mode with cable compensation.

In this case the filter coefficients will include the standard cable compensation.
Manual Mode without Cable Compensation

This mode allows configuring the filter coefficients directly. No additional cable compensation is being done.

**NOTE**

Note that when switching from Preset mode to Manual mode without cable compensation, the filter coefficients are not cleared to default. This way, the setting of the Preset mode can be taken over and fine-tuned manually.
Automatic Equalizer Coefficient Optimization

The M8046A provides an automatic optimization of the equalizer coefficients.

The automatic optimization can only be used when the individual cursor coefficients are controllable. If the equalizer is operated in preset mode, it will automatically switch to manual mode without cable correction before starting optimizing the equalizer setting.

Precondition:

- The received signal must contain all symbol levels according to the line coding being used.
- The optimization will fail, if a PAM4 signal is only containing 2 or 3 out of the possible 4 symbol levels.
- The received signal must produce distinguishable peaks for the signal levels and at least some ‘valley’ between the peaks.
- The equalizer auto set function includes finding the corresponding sample delay setting. But the sample delay will be re-programmed to the initial value after the equalizer setting has been determined.
- The input range needs to be configured correctly.
  Use the Input Range auto-set function to configure the Input Range to the correct value.

When the pre-conditions are met, the equalizer auto-set can be executed. Performing the full auto-alignment after the equalizer optimization, will set the sample delay and thresholds to the best possible delay setting.

Using the equalizer auto-set

- Open the Sample Point Setup window.
  The individual steps can also be done from the Parameters window, but the Sampling Point Setup provides the response on the progress and display quality results of the settings.

- Press to optimize the Input Range

- Press to optimize the equalizer coefficients

- Press to determine the optimum sample delay and threshold settings
Manual Optimization of the Equalization Level in Preset Mode

The sampling point setup is showing histogram data of the received signal for an M8046A error detector. This can be used to determine the required equalization level.

1. Go to Menu Bar > Analyzer and then select Sampling Point Setup.
2. Click on the **Parameters** tab on the right side of the graph. Ensure that the parameters remain visible by clicking the pin at the top right corner.
3. Start with the maximum Input range of 500 mV. This ensures that the received signal will not get clipped in the input stage.

4. Click the sample delay marker, and keep the left mouse button held down, while dragging the marker to a position that is supposed to be between the transitions of the signal. Alternatively change the sample delay setting in the parameter editor.

This does not have to be perfect, the goal is just not to sample at the signal transitions.
5. Adjust the input range so that the signal is using around 90 to 95 percent of the input voltage window.
6 Increase the equalization level while observing the histogram. Find the equalization level that opens the eye. This may require re-adjusting the sample delay marker.
7 After manually optimizing the sample delay.

8 It may be required to iterate steps 6 and 7.
9 Finally, click the auto-alignment button.
In this example the received signal is a PAM4 signal with a peak amplitude of 150 mV and completely closed eyes. The auto alignment reports eye heights of 10 mV, 9 mV and 13 mV in the logger (Utilities > Logger) for an alignment BER threshold of 1e-9. At the end of the auto alignment, the sampling point setup will draw a schematic eye diagram that gives an indication of the eye opening at the configured alignment BER threshold.

The above figure shows the calculated threshold values and the black area at the sampling point shows the total eye opening achieved after applying equalization.

**NOTE**

The alignment BER threshold defines the BER level that is used by the auto-alignments to determine the inner eye opening as shown in the sampling point setup. The inner eye opening at the alignment BER threshold is used to calculate the optimum sample delay and threshold voltages. The lower BER alignment threshold values result in a more precise sampling point, especially when the eye opening is small. It also increases the measurement execution time.
Pattern Synchronization

The M8020A/M8030A/M8040A calculates bit error rates by comparing the received data with the expected data patterns. To do this, it needs to know where the start of the pattern is located in the data stream.

Introduction to Pattern Synchronization

Pattern synchronization (sync) refers to aligning the incoming data pattern with the internal reference pattern.

Hardware-Generated Patterns

For 2^n-1 PRBS patterns, bits from the incoming data pattern "seed" the Analyzer's Generator, causing it to generate a precisely aligned internal reference pattern.

Memory-Based Patterns

For software-generated and user patterns, a 48-bit pattern from the pattern is used as a detect word. Optimally, this detect word should be unique within the entire pattern. The Analyzer searches for this detect word within the incoming data stream, and uses the point in the data stream as a reference, and compares all following bits with the pattern. If the measured BER is better than the synchronization BER, the Analyzer will be synchronized.

There are thus three possible outcomes for a synchronization:

- Single instance of the detect word in the data stream
• Multiple instances of the detect word with correct synchronization.

• Multiple instances of the detect word with false synchronization.
If the Analyzer attempts to synchronize on the incorrect detect word, the BER will be unacceptably high, and, if automatic synchronization is selected, the Analyzer attempts another re-sync.

The detect word on which the Analyzer attempts to re-sync is chosen strictly by chance. So if there are two instances of the detect word in the pattern, the Analyzer has a 50% chance of selecting the correct one.

The more instances of the detect word exist in the pattern, the higher are the chances for incorrect synchronization. The software attempts in any case to identify a 48-bit pattern that occurs as seldom as possible in the pattern. For very large patterns, this can unfortunately take a very long time, and the software ends the search if it expects that it would take longer to find an adequate detect word than it would to attempt to synchronize. If the search for a detect word is ended, the most unique detect word identified is used.

Patterns must always be synchronized in order to do accurate BER testing. If patterns are out of alignment by just one bit, errors can be as high as 50% (5E-1) for PRBS patterns, and 100% (1E+0) for custom patterns.
By default, the Analyzer is in automatic sync mode with a sync threshold of 1E-3. This setting is recommended for most applications, and usually allows the synchronization function to be “transparent”, requiring no attention. However, for special applications, changes can be made to the sync mode and sync threshold.

What Type of Synchronization Should You Use?

The type of synchronization you use affects how errors are measured and displayed. A Sync Loss is recognized when the BER is greater than the sync threshold. This can be caused by a high error rate, pattern misalignment, or clock loss. Choose the sync mode setting that is appropriate for the type of errors you anticipate.

- Automatic Sync with a sync threshold BER of 1E-3 is recommended for most applications.
  
  With this mode selected, the synchronization algorithm starts whenever the BER exceeds the threshold. However, it is not possible to make accurate BER measurements higher than the sync threshold.

- Manual sync can be used for synchronizing once, confirming proper pattern alignment, and then measuring BERs higher than the sync threshold. This is useful for the following applications:
  
  - To monitor the integrity of clock signals. You may wish to measure BERs that exceed the sync threshold to confirm clock slip.
  - To collect data for constructing eye contour information. You may wish to move the sampling point to locations in the data eye that have BERs exceeding the sync threshold.

  This mode doesn't allow the analyzer to automatically synchronize if the BER becomes greater than the sync threshold. For example, the analyzer will not re-synchronize after momentary clock loss.

**NOTE**

Adjusting the data input delay may cause momentary clock loss. If you select Manual Sync mode, this may also result in sync loss.

- Burst sync mode is a special operating mode for measuring data in bursts of bits, rather than one continuous stream of bits.
What is False Synchronization?

For patterns other than PRBS, the **Analyzer** may gain sync at a point in the pattern that meets the sync threshold, but is not the correct point where the internal reference pattern and the received data pattern match. This is called false synchronization.

**NOTE**

False synchronization cannot occur with PRBS patterns because a 1 bit misalignment would cause a measurement of 50% or more errors. Thus, the BER during a misalignment would always be greater than the sync threshold BER.

For example, consider a pattern of 1000 ones and 1000 zeros as shown in the following figure. With reference alignment 1 the patterns are totally out of phase and the Analyzer is measuring 100% errors.

But as the reference moves closer to optimum alignment, the percentage of errors gradually approaches zero (reference alignment 2 and 3). For exact alignment, the sync threshold must be set lower than the BER caused by a 1 bit misalignment, in this case 1E-3.
How Can You Tell if Your Synchronization is False?

You may suspect false synchronization under the following conditions:

- You are using a pattern other than PRBS and the Analyzer gains sync, but it measures a constant, fixed error ratio.
- You are using a pattern other than PRBS and the Analyzer gains sync, but auto-search functions (Auto Align, Clock/Data Center, Threshold Center) repeatedly fail.

In a false sync, the sync threshold BER of 1E-3 may be met, but eye edges at BER 1E-3 (required by an auto-search function) may not be found. This is because BERs less than 1E-3 do not exist within the data eye.
If you suspect a false sync, try re-synchronizing at a sync threshold BER lower than the fixed error ratio. If sync is acquired without the problems listed above, then your previous sync was false. Your current sync should be on an exact pattern alignment.
How to Synchronize an Incoming Pattern

To synchronize the incoming pattern to the expected pattern:
1. Go to the Menu Bar > Analyzer and then select Data In.
2. Select the Analyzer function block from the Parameters window.
3. Select Re-Sync. The choices are Automatic or Manual.
   - Automatic Sync
     When this option is selected, the Analyzer constantly tries to synchronize the patterns when the BER threshold is exceeded.
   - Manual
     Manual synchronization can be selected, for example, if the signal delay is very unstable, and you want to avoid that, the resynchronization process affects the measurement results.

NOTE

While auto-search functions are in progress, the sync threshold BER is changed to the same value as the alignment BER threshold. If you are using these functions and want to consistently re-synchronize at a lower sync threshold, you must set the alignment BER threshold to the same value as the sync threshold BER.
Bit Recovery Mode

Understanding Bit Recovery Mode (BRM)

The M8040A analyzer (M8046A) does not support bit recovery mode.

Traditionally, bit error rate testing compares the bits from a Device Under Test (DUT) against a reference data set, called the expected data. The user of Bit Error Rate Tester (BERT) has to provide this expected data and load it into the M8020A/M8030A.

The M8020A/M8030A system then samples the incoming data signal with a sampling point that can be varied over time and voltage, to measure the BER. The M8070B system software is capable of creating graphics, such as the eye opening, from the information gathered during sampling. A compare circuit counts the differences between the bits of the incoming data stream and the expected data.

Now there is a mode that removes the need for the user to provide expected data, while still allowing one and two-dimensional measurements, such as the eye opening.

This is the Bit Recovery Mode (BRM).

This has two benefits:

- the user does not need to worry about the expected bits, which makes a setup easier and faster.
- the M8020A/M8030A system can measure non-deterministic data streams. This means it is no longer necessary to force a device into a specific test mode.

Bit recovery mode uses a second sampling circuit in the M8020A/M8030A analyzer to always sample at the sweet spot of the eye (typically at 50% of eye opening in time and voltage). The sampled data from this second sampling circuit acts as a reference and is passed to the compare circuitry, instead of the expected data.

This means the BER is now a relative figure. Taking the bit from the sweet spot of the eye cannot verify if this bit is correct in itself, it can just use it as a reference for any bit sampled in the border area of the eye. Bit recovery mode makes one and two-dimensional sweeps possible to sample in the border area of the eye and find out how the BER value increases. From this
we can derive the random and deterministic (Rj and Dj) characteristics.

We can also take the eye opening with a known, deterministic test pattern and compare it with operational data, where a device idles or provides scrambled data, or there are asynchronous events like hand-shake signals.

The Bit Recovery mode also has a limitation that it requires a minimum eye opening: an eye that is too narrow cannot be processed. Care also needs to be taken if there is a good eye opening but there is a finite BER inside the eye.

Setting up Bit Recovery Mode

To set up the Bit Recovery Mode mode:

1. Go to the Menu Bar > Analyzer and then select Data Input or if you are in Module View, then click on Data In location.
2. Select Analyzer functional block from the Parameters window.
3. Click Bit Recovery Mode switch to turn on the Bit Recovery Mode.

Once the Bit Recovery Mode is enabled, the BRM indicator on the Status Indicator turns green. See Status Indicators Window on page 107.

BRM can be used with all measurements supported by M8070B system software.
Line Coding

You can define the line coding for a Data In port of the M8046A module through the Parameters window.

To set the line coding:
1. Go to the Menu Bar > Generator and then select Data In.
2. Select Line Coding functional block from the Parameters pane.
3. Select the line coding. The Data In port supports NRZ and PAM4 line coding which defines how consecutive data bits are mapped to symbols.

The PAM4 line coding provides the following symbol mapping options:
- **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 01 maps to symbol 1, 10 maps to symbol 2 and 11 maps to symbol 3.
- **Gray Coded** - In this mapping, the bit sequence 00 maps to symbol 0, 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.
- **Custom** - In this mapping the consecutive data bits are mapped to symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10). The position within this list corresponds to the symbol level. First value is for Symbol 0 and the last value is for Symbol 3.
Alignment Results

The alignment results are the output of auto alignment. These results are displayed on pressing the auto-alignment button.

The following alignment results are available for NRZ coding:

- **Eye Width** - Width of the eye opening
- **Delay** - Optimum sample delay
- **Input Range** - Input voltage range
- **Threshold** - Optimum threshold voltage
- **Polarity** - Data polarity used for pattern synchronization

The following figure illustrates alignment results for NRZ coding:

![Alignment Results Table](image)

The following alignment results are available for PAM4 coding:

- **Eye Width** - Width of the eye opening
- **Delay** - Optimum sample delay
- **Input Range** - Input voltage range
- **Upper Threshold** - Upper PAM4 decision threshold
- **Middle Threshold** - Middle PAM4 decision threshold
- **Lower Threshold** - Lower PAM4 decision threshold
- **Polarity** - Data polarity used for pattern synchronization
The following figure illustrates alignment results for PAM4 coding:

![Alignment Results Table]

<table>
<thead>
<tr>
<th>Alignment Results</th>
<th>M2.DataIn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Width</td>
<td>151.4 ps</td>
</tr>
<tr>
<td>Delay</td>
<td>137.4 ps</td>
</tr>
<tr>
<td>Input Range</td>
<td>357 mV</td>
</tr>
<tr>
<td>Upper Threshold</td>
<td>67 mV</td>
</tr>
<tr>
<td>Middle Threshold</td>
<td>-12 mV</td>
</tr>
<tr>
<td>Lower Threshold</td>
<td>-78 mV</td>
</tr>
<tr>
<td>Polarity</td>
<td>Non-Inverted</td>
</tr>
</tbody>
</table>
7 Setting up Patterns

Pattern Overview / 388
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Using M8062A Data Out Squelch Feature / 498
M8046A PHY Protocol Selection (SKP OS Filtering) / 502
Pattern Overview

The purpose of data patterns is to simulate the type of data that your device might receive in the real world. Different patterns present different data loads to your instrument, which can cause variations in the bit error ratio. A bit pattern is sent from the generator to your device. At the same time, the expected output pattern of your device is internally generated in the analyzer (to provide a reference).

The M8041A and M8051A modules support 2 Gb pattern memory per channel (requires M8070B).

The M8045A and M8046A modules support 2 Gb pattern memory per channel (requires M8070B)

Selecting a pattern is the first step in setting up a BER measurement. The M8020A/M8030A provides various patterns to fulfill most standard testing needs. The M8020A/M8030A modules support the following types of patterns:

• PRBS
• Pulse
• Clock
• Static
• Memory Patterns

The M8040A modules support the following types of patterns:

• PRBS (supports all except for 2^7-1 on analyzer)
• Pulse (supports for NRZ, doesn’t support for PAM4)
• Clock (supports for NRZ, doesn’t support for PAM4)
• Static
• Memory Patterns

Patterns consist of a sequence of symbols. A symbol can have the following type of coding:

• Binary (Bit)
• 8B/10B
• 128B/130B
• 128B/132B
Sequence Editor

Overview

The sequence editor allows you to create and maintain sequences. In addition to this, it also allows you to edit the memory patterns.

A sequence consists of up to 500 blocks that can be looped. Single or multiple blocks can be looped. The sum of the blocks and the counted loops must not exceed 500. An overall loop restarts the sequence after it has come to its end.

You can also upload predefined sequences for PCIe, USB and SATA using the Recall Setting dialog. For details, refer to Recall/Save Instrument State on page 118.

When to Use a Sequence

You may wish to test a device that uses a certain protocol for processing data.

For example, the device might expect synchronization data, a preamble, payload data, and a suffix.

All this can be provided by a user-defined sequence.

How a Sequence is Defined

The sequence is defined by a SequenceExpression which is formulated in its own language, checked by the Sequence Editor.

The SequenceExpression specifies:
- the sequence start (and break) conditions
- the blocks, their contents, and trigger output
- the loops
How to Launch a Sequence Editor

To launch the **Sequence Editor**:

- Go to the **Menu Bar > Patterns** and then select **Sequence Editor**.

The **Sequence Editor** will appear as shown in the following figure:

![Sequence Editor Interface](image)

The **Sequence Editor** user interface includes the following elements:

- Toolbar
- Sequence Control Pane
- Sequence Settings Window
- Pattern Edit Pane

These GUI elements are described in the section that follows.
The toolbar provides the following convenient sequence editing functions:

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>![New]</td>
<td>New</td>
<td>Click this icon to create a new sequence. Refer to Creating New Sequence on page 392.</td>
</tr>
<tr>
<td>![Download]</td>
<td>Download</td>
<td>Click this icon to save the modifications that are done using the Sequence Settings window on the module.</td>
</tr>
<tr>
<td></td>
<td>An orange icon</td>
<td>An orange icon indicates that modifications are not yet applied on the module. You can also apply the changes on either generator, or analyzer or both.</td>
</tr>
<tr>
<td>![Reload]</td>
<td>Reload Running Sequence</td>
<td>Click this icon to reload the running sequence settings. Reloading a sequence will discard the changes made in the sequence editor and will reload the current sequence with its factory settings.</td>
</tr>
<tr>
<td>![Add Block Before]</td>
<td>Add Block Before</td>
<td>Click this icon to add a block before selected sequence block.</td>
</tr>
<tr>
<td>![Add Block After]</td>
<td>Add Block After</td>
<td>Click this icon to add a block after selected sequence block.</td>
</tr>
<tr>
<td>![Loop]</td>
<td>Loop</td>
<td>Click this icon to create a loop in a sequence block. Refer to Creating a Loop on page 395.</td>
</tr>
<tr>
<td>![Delete]</td>
<td>Delete</td>
<td>Click this icon to delete the selected block from the sequence. Deleting a block will also remove all loops that are associated with this block.</td>
</tr>
<tr>
<td>![xml]</td>
<td>Click this icon to toggle between the user interface and xml code. The changes made in user interface are also reflected in xml code and vice versa.</td>
<td></td>
</tr>
<tr>
<td>![Show Patterns]</td>
<td>Shows the patterns in the Pattern Edit Pane if the selected block has memory patterns.</td>
<td></td>
</tr>
</tbody>
</table>
Setting up Patterns

Creating New Sequence

To create a new sequence:

1. Click on the **Create New Sequence** icon present on the toolbar. A **Create New Sequence** dialog will appear which allows you to create a new sequence.

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Break</td>
<td></td>
<td>Click this icon to terminate an infinite loop that is set to &quot;manual&quot; break condition. Sequence execution continues with the next block.</td>
</tr>
<tr>
<td>Reset</td>
<td></td>
<td>Click this icon to interrupt and re-initialize a running sequence.</td>
</tr>
<tr>
<td>Sync</td>
<td></td>
<td>Click this icon to sync the sequences globally.</td>
</tr>
<tr>
<td>Import Sequence</td>
<td></td>
<td>Click this icon to import a sequence. For details, refer to Importing a Sequence on page 393.</td>
</tr>
<tr>
<td>Export Sequence</td>
<td></td>
<td>Click this icon to export a sequence in the desired location. For details, refer to Exporting a Sequence on page 395.</td>
</tr>
</tbody>
</table>
2 Perform the following settings:
   - **Name** - Provide a sequence name.
   - **Description** - Provide a description of the sequence.
   - **No. of Blocks** - Enter the number of blocks to be added. You can add up to 500 blocks in a sequence.
   - **Locations** - Click on the button to open the **Select Sequence Locations** dialog box. Use this dialog box to select the sequence location. You can either select a single sequence location or multiple locations.

3 Click **Create** to create a sequence.

Importing a Sequence

The M8070B **Sequence Editor** allows you to import the sequences, edit them and then use them for testing and analysis.

To import a sequence:
1 Click the **Import Sequence** icon. This opens the standard Windows **Open** dialog, where you can locate the sequences.
Please note that you are only allowed to import patterns with .m8ks file extension.

2 Click Open. A Import Sequence dialog will appear as shown in the following figure:

![Import Sequence dialog](image.png)

This dialog allows you to select the following sequence and pattern options:

a **Select sequence to import**: Select the check box to import the sequences from generator, analyzer or both.

b **Sequence Options**: Select the check box to delete existing sequences, use location of the imported sequences and download sequence after importing.

c **Pattern Option**: Select this option to also import the patterns used in the selected sequences.

3 Click OK to import the sequences.

Please note that the selected sequences with the same name will be overwritten.
Exporting a Sequence

The M8070B Sequence Editor allows you to export patterns and use it for testing and analysis.

To export a pattern:

1. Click the Export Sequence icon. This opens the Export Sequence dialog which allows you to export the sequences from Generator, Analyzer or both. Additionally, it also allows you to export the patterns used in the sequences.

2. Click OK. A standard Windows Save As dialog will open which allows you to save the sequence under the defined file name and location.

Creating a Loop

To create a loop (if desired):

- Click the Add Block Before icon to add the blocks before the selected sequence blocks.
- Click the Add Block After icon to add the blocks after the selected sequence blocks.
Click the Create Loop icon. A Create Loop dialog will appear as shown in the following figure:

![Create Loop dialog](image)

- Specify the start and end block of the loop for the specified sequence (for e.g. generator, analyzer or user-defined sequence).
- Click Create to create a loop in the specified blocks.
- Click on the loop indicator. You will see a Loop Setting functional block in the Sequence Setting window where you can specify the loop count and enable the looping option.

**Loop Within Sequences**

A loop defines the transition from the end of a block to the beginning of the same or a previous block. It is not possible to jump into an existing loop. It is also not possible to specify loops within loops (except the default overall loop).

For information on how to create a loop, refer to Creating a Loop on page 395.

**Deleting a loop** - It is possible to delete a loop. To delete a loop, select the loop indicator and click Delete icon.

**Modifying the Existing Sequences**

By default, the Generator and Analyzer sequences already exist whenever you launch a Sequence Editor. You can however modify these sequences as per the requirements. Using these options, you can:

- Add and delete the blocks
- Add loops in the blocks
- Specify the settings for each block using the Sequence Settings window. For more details, refer to Sequence Setting Window on page 397.
Once the settings are done, click the Download icon to apply the sequence settings either on generator or on analyzer or on both.

**NOTE**
Please note that there should be at least one block in the sequence.
Remember that you are not allowed to perform delete operation in the block if there is only one block in sequence.

Sequence Setting Window

The **Sequence Setting** window allows you to set the properties for the selected block and sequence. Using this window, you can specify the following settings:

- **Instrument Configuration.** For details, refer to Instrument Configuration on page 398.
- **Sequence Configuration.** For details, refer to Sequence Configuration on page 410.
- **Link Training Configuration.** For details, see Link Training Configuration on page 401
- **Block Data.** For details, refer to Block Data on page 411.
- **Block Settings.** For details, refer to Block Settings on page 414.
- **Block Branches.** For details, refer to Block Branches on page 415.
- **Block Controls.** For details, refer to Block Controls on page 416.

**Set to Default Check-Box**

Most of the parameters in the **Sequence Setting** window contains a **Set to Default** check-box which gets highlighted when some modifications are done. You can click on this check-box to change the settings to their default values.

The following figure shows how the check-box gets highlighted when you modify the symbol width to 10.

![Set to Default Check-Box](image)

However, when you click on the **Set to Default** check-box, the value changes to 1 (default value). See the following figure.
Instrument Configuration

The instrument configuration section provides the following options:

- **Symbol Width**: Use this option to select the symbol width e.g., 1, 10, 130 or 132 bit. Depending upon the symbol width you have selected, you can specify the coding configuration for that particular symbol width.

- **Replicate**: Select the replicate option (Serialized, Copy or Copy plus Phase Adjust).

If the symbol width is 10, you can specify the 8B/10B coding configuration. Using this, you can define alignment symbol, replacement symbol and filler primitives.

The **Alignment Symbol** contains the K28.1, K28.5 and K28.7 symbols.
The **Replacement Symbol** contains the K28.0, K28.4, K28.7, K23.7, K27.7, K29.7 and K30.7 symbols.

**Filler Primitives** are inserted or deleted for clock tolerance compensation. These are not compared and therefore cannot be counted as errors. **Filler Primitives** contain symbols. A maximum of four alternative filler primitives can be used. Each filler primitive can consist of up to 4 filler symbols. Filler symbols are separated by comma (,). To add filler primitive:

- Click the **Add Primitive** button.
- Enter the **Symbol**. The filler primitive can consist of up to 4 filler symbols.

![Filler Primitives](image)

**Wild Cards for Filler Primitives**

The wild cards allow you to set one or more out of the maximum of four symbols of a filler primitive as don’t care. In this case, all allowed D and K symbols will match and are removed from incoming DUT data.

For example:

K28.5, *

Here the dot (•) symbol will be treated as don’t care.

**Add Scrambler Configuration**

Select the **Scrambler Configuration** check-box to add scrambler configuration to the sequence.
7 Setting up Patterns

It allows you to:
• Reset Primitive
• Hold Primitive
• Pause Start Primitive
• Pause End Primitive
• Polynomial
• Reset After Filler Remove
• Reset Value
• Reset Value After Hold

If the symbol width is 130, you can specify the 128B/130B coding configuration. Using this, you can define scrambler reset value and EIEOS (Electrical Idle Exit Ordered Set) for PCIe3 or PCIe4.
PCIe/USB/SATA Scrambler Polynomials

For the symbol width 8b/10b, the following scrambler polynomials are used:

- **PCIe/USB** - \( G(x) = x^{16} + x^5 + x^4 + x^3 + 1 \)
- **SATA** - \( G(x) = x^{16} + x^{15} + x^{13} + x^4 + 1 \)

For the symbol width 128b/130b and 128b/132b, both standards use the same scrambler polynomial as following:

- **PCIe/USB** - \( G(x) = x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1 \)

Link Training Configuration

This section allows you to configure link training for USB 3.0, USB 3.1, PCIe 3.0 and PCIe 4.0 and PCIe 5.0.

**Link Training for USB 3.0 and USB 3.1**

The M8070B system software allows you to test the physical layer compliance of a USB 3.0 and USB 3.1 DUT. It provides the parameters which can be configured for link training USB 3.0 and USB 3.1.

If the symbol width is 10, you can configure the link training parameters for USB 3.0 to control LTSSM (Link Training and Status State Machine). However, if the symbol width is 132, you can configure the link training parameters for USB 3.1 to control LTSSM.

The following figure shows the parameters which can be configured for link training USB 3.0:
The following parameters are available to configure link training USB 3.0:

- **DUT Type** - Specifies which role the BERT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.
- **Target State** - Determines the target state when bringing up the link.
- **Trigger State** - This parameter determines when the trigger output signal of the LTSSM block should be asserted. Additionally, this information can be translated into a trigger pulse on entering or leaving the specified state. This is done by the pulse shaper of the TCRL OUT connector and no direct functionality of the LTSSM.
- **LFPS tPeriod** - Period of the LFPS cycle.
- **LFPS Duty Cycle** - Duty cycle of the LFPS cycle.
- **Polling LFPS tBurst** - Link Training handshake before 5Gb/s.
- **Polling LFPS tRepeat** - Link Training handshake before 5Gb/s.
- **Warm Reset LFPS tBurst** - LFPS triggers transition to Rx.Detect.

The following figure shows the parameters which can be configured for link training USB 3.1:
The following parameters are available to configure link training USB 3.1:

- **DUT Type** - Specifies which role the BERT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.
- **Target State** - Determines the target state when bringing up the link.
- **Trigger State** - This parameter determines when the trigger output signal of the LTSSM block should be asserted. Additionally, this information can be translated into a trigger pulse on entering or leaving the specified state. This is done by the pulse shaper of the TCRL OUT connector and no direct functionality of the LTSSM.
- **LFPS tPeriod** - Period of the LFPS cycle.
- **LFPS Duty Cycle** - Duty cycle of the LFPS cycle
- **Warm Reset LFPS tBurst** - LFPS triggers transition to Rx.Detect.
- **SCD1 and SCD2** - SuperSpeedPlus Capability Declaration (SCD) is a step for a SuperSpeedPlus port, while in the Polling. LFPS substate, to identify itself as SuperSpeedPlus capable by transmitting Polling LFPS signals with specific patterns unique to SuperSpeedPlus ports.
• **SuperSpeedPlus LFPS Based PWM Message (LBPM)** - LBPM is defined as a low power signaling mechanism for two SuperSpeedPlus ports to communicate with each other based on LFPS signals. The adoption of Pulse Width Modulation (PWM) is to embed the transmitting clock in data and to allow for easy data recovery at the receiver based on LFPS clock.

For further details on link training for USB 3.0 and USB 3.1, refer to Interactive Link Training on page 466.

**Link Training PCIe 3.0, PCIe 4.0 and PCIe 5.0 Parameters**

The M8070B system software allows you to test the physical layer compliance of a PCIe 3.0, PCIe 4.0 and PCIe 5.0 DUT. It provides the parameters which can be configured for link training PCIe 3.0, PCIe 4.0, and PCIe 5.0.

In case of M8020A, if the symbol width is 130, you can configure the link training parameters for PCIe 3.0 and PCIe 4.0 to control LTSSM (Link Training and Status State Machine).

In case of M8040A, the interactive link training functionality is specified differently by selecting a PHY Protocol from the Sequence Configuration block. For more details, see M8070B Support for PCIe3.0/4.0/5.0 Link Training using M8040A on page 485.

The following figure shows the parameters which can be configured for link training PCIe 3.0:
The following parameters can be configured as an attributes.

- **EIEOS** - The EIEOS (Electrical Idle Exit Ordered Set) allows you to choose the pattern (PCIe3 | PCIe4) to be used for link training.
- **Generation** - Specifies the target link training PCIe Gen3 (8GT/s) or PCIe Gen 4 (16GT/s).
- **DUT Type** - Specifies which role the DUT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.
- **Clock Architecture** - Specifies the clock architecture whether common or separate. In case of common clock, a common RefClk is expected. The M8000 instrument and the DUT run on the same clock. The RefClk is provided by the ‘Trig Out’ of the clock module of the M8000 instrument. In case of separate clock, the DUT runs on its own RefClk provided by itself or by an external source. The ‘Trig Out’ of the M8000 instrument is not used as RefClk for the DUT.
• **Loopback through** - Specifies if the real-time equalization is done while going into loopback through LO / Recovery or through Configuration. When selecting Loopback through LO-Recovery, the LTSSM does a link training as before. Selecting Loopback through Configuration does a link training without real time equalization. When the Loopback through Configuration is selected, all preset parameters are disabled.

• **Trigger State** - Specifies the trigger state. It can be an Add-in-Card (AIC) or a root- complex.

• **Lane** - Specifies the lane number being used.

• **Link** - Specifies the link number being used.

• **Compliance Receive Bit** - Specifies whether the compliance received bit is asserted or deasserted.

• **Link Equalization** - Determines whether link equalization should be performed. It can either be aborted after phase 1 (Bypass) or fully executed. In the second case it can be determined whether only preset or all (i.e. individual cursor) requests should be accepted.

• **Start Preset** - Specifies the preset used by the J-BERT’s TX port after switching to Gen 3 operation and when operating as an upstream device.

• **DUT Preset Hint** - Specifies the preset hint being sent by the J-BERT to the DUT during phase 0 of the link equalization procedure. It is only used when the BERT operates as upstream device.

• **DUT Initial Preset** - Specifies the preset the J-BERT transfers to the DUT in phase 0 of the link equalization procedure. It is only used when the BERT operates as an upstream device.

• **DUT Target Preset** - Specifies the preset the J-BERT requests the DUT to switch to during link equalization. Depending on the role the J-BERT is playing, this is done in either phase 2 or 3 of the link equalization training.

• **Speed Change Control** - Specifies whether the speed change to Gen3 (i.e. 8 Gbps) speed will be initiated by DUT or BERT during link training. It is only used when the BERT operates as a downstream device. If not specified DUT will initiate the speed change and will also request BERT for the same. It is only used for the DUT type as System Board.

• **User Calibrated Presets** - Specifies whether BERT’s Data Out should use user-calibrated presets or standard presets during link training. Enabling it means that BERT’s Data Out will use de-emphasis/pre-shoot values that had been previously calibrated, otherwise it will use standard de-emphasis/pre-shoot values defined by the PCIe3 specification. By default this option is turned off which means that standard presets will be used.
For further details on link training for PCIe 3.0, refer to *Interactive Link Training* on page 466.

The following figure shows the parameters which can be configured for link training PCIe 4.0:

The following parameters can be configured as an attributes.

- **EIEOS** - The EIEOS (Electrical Idle Exit Ordered Set) allows you to choose the pattern (PCIe3 | PCIe4) to be used for link training. Electrical Idle Exit Ordered Set (EIEOS) for 8.0 GT/s Data Rates
Electrical Idle Exit Ordered Set (EIEOS) for 16.0 GT/s Data Rates

<table>
<thead>
<tr>
<th>Symbol Numbers</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0, 2, 4, 6, 8, 10, 12, 14</td>
<td>00h</td>
<td>Symbol 0: EIEOS Identifier. A low frequency pattern that alternates between eight 0s and eight 1s.</td>
</tr>
<tr>
<td>1, 3, 5, 7, 9, 11, 13, 15</td>
<td>FFh</td>
<td>A low frequency pattern that alternates between eight 0s and eight 1s.</td>
</tr>
</tbody>
</table>

- **Generation** - Specifies the target link training PCIe Gen3 (8GT/s) or PCIe Gen 4 (16GT/s).
  
  If Gen 4 is selected:
  
  DUT Target Preset -Cursor is not available in this case for Gen 3
  DUT Target Preset (Gen4) - Cursor can be used instead only for Gen 4

- **DUT Type** - Specifies which role the DUT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.

- **Clock Architecture** - Specifies the clock architecture whether common or separate. In case of common clock, a common RefClk is expected. The M8000 instrument and the DUT run on the same clock. The RefClk is provided by the ‘Trig Out’ of the clock module of the M8000 instrument. In case of separate clock, the DUT runs on its own RefClk provided by itself or by an external source. The ‘Trig Out’ of the M8000 instrument is not used as RefClk for the DUT.

- **Loopback through** - Specifies if the real-time equalization is done while going into loopback through L0 / Recovery or through Configuration. When selecting Loopback through L0-Recovery, the LTSSM does a link training as before. Selecting Loopback through Configuration does a link training without real time equalization. When the Loopback through Configuration is selected, all preset parameters are disabled.
• **Trigger State** - Specifies the trigger state. It can be an Add-in-Card (AIC) or a root-complex.
• **Lane** - Specifies the lane number being used.
• **Link** - Specifies the link number being used.
• **Compliance Receive Bit** - Specifies whether the compliance received bit is asserted or deasserted.
• **Link Equalization** - Determines whether link equalization should be performed. It can either be aborted after phase 1 (Bypass) or fully executed. In the second case it can be determined whether only preset or all (i.e. individual cursor) requests should be accepted.
• **Start Preset** - Specifies the preset used by the J-BERT’s TX port after switching to Gen 4 operation and when operating as an upstream device.
• **DUT Preset Hint** - Specifies the preset hint being sent by the J-BERT to the DUT during phase 0 of the link equalization procedure. It is only used when the BERT operates as an upstream device.
• **DUT Initial Preset** - Specifies the preset the J-BERT transfers to the DUT in phase 0 of the link equalization procedure. It is only used when the BERT operates as an upstream device.
• **DUT Target Preset** - Specifies the preset the J-BERT requests the DUT to switch to during link equalization. Depending on the role the J-BERT is playing, this is done in either phase 2 or 3 of the link equalization training.
• **Select Start Preset Gen 4** - User Defined
  Defines which values to be used as Start Preset Gen4
  · User Defined - Start Preset (Gen 4) entered by user.
• **Start Preset Gen 4** - Start Preset Gen 4 value entered by user (P0 – P9).
• **DUT Initial Preset Gen 4** - DUT Initial Preset Gen 4 value entered by user (P0 – P9).
• **DUT Target Preset Gen 4** - DUT Target Preset Gen 4 value entered by user (P0 – P9, Cursor)
• **User Calibrated Presets** - Specifies whether BERT’s Data Out should use user-calibrated presets or standard presets during link training. Enabling it means that BERT’s Data Out will use de-emphasis/pre-shoot values that had been previously calibrated, otherwise it will use standard de-emphasis/pre-shoot values defined by the PCIe3 specification. By default this option is turned off which means that standard presets will be used.

For further details on link training for PCIe 4.0, refer to **Interactive Link Training** on page 466.
Sequence Configuration

The sequence configuration section provides the following options:

- **Sequence**: Allows you to apply a sequence configuration on either Generator, Analyzer or user-created sequences.
- **Name**: Provide the sequence name.
- **Locations**: Specify the locations for the sequence. Use the button available to select the locations.
- **Replicate**: Select the replicate option (Serialized, Copy or Copy plus Phase Adjust).
- **Description**: Add a description to the sequence.

**NOTE**

Make sure not to use the unused location which are not being used in the test setup. However, if it is used, ensure that the 'Re-Sync' parameter of these locations is set to manual to reduce overall system load caused by unnecessary pattern re-sync attempts.
Block Data

The Block Data section allows you to:

- Provide a block name.
- Provide a block length.
- Select Block Type. The available options are Clock, Pulse, PRBS, Static, Memory Pattern and Link Training.
  
  - For block type as Clock, you need to specify the Divider, Replicate and the Compare feature (refer Compare Feature on page 414).
  
  - The Replicate feature shows how the serial patterns are split to multiple locations. It has the option options:
    
    Serialize: In this a pattern is split and distributed to the locations. This is for the parallel side of a serial bus.
    
    Copy: In this each location gets a copy of the pattern.
    
    Copy Plus Phase Adjust: In this each location gets a copy of the pattern. Scrambler phases of the different locations are set differently. This is for the parallel side of a serial bus.
  
  - For block type as Pulse, you need to specify the Width, Compare and Offset feature.
  
  - For block type as PRBS, you need to specify the Polynomial, Replicate, Invert and Seed (Hex) feature. Refer to the Table 51 on page 412 and Table 52 on page 413 for the list of available PRBS polynomials.
The following tables shows the PRBS polynomial for M8020A/M8030A/M8040A that is used to generate the selected PRBS $2^n-1$.

Table 51  PRBS polynomials for M8020A/M8030A/M8040A

<table>
<thead>
<tr>
<th>PRBS</th>
<th>Shift Register Length</th>
<th>Polynomial</th>
<th>PRBS Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2^7-1$</td>
<td>7</td>
<td>$x^7\cdot x^6+1$</td>
<td>127</td>
</tr>
<tr>
<td>$2^9-1$</td>
<td>9</td>
<td>$x^9\cdot x^5+1$</td>
<td>511</td>
</tr>
<tr>
<td>$2^{10}-1$</td>
<td>10</td>
<td>$x^{10}\cdot x^7+1$</td>
<td>1023</td>
</tr>
<tr>
<td>$2^{11}-1$</td>
<td>11</td>
<td>$x^{11}\cdot x^9+1$</td>
<td>2047</td>
</tr>
<tr>
<td>$2^{13}-1$</td>
<td>13</td>
<td>$x^{13}\cdot x^{12}\cdot x^2+1$</td>
<td>8191</td>
</tr>
<tr>
<td>$2^{15}-1$</td>
<td>15</td>
<td>$x^{15}\cdot x^{14}+1$</td>
<td>32767</td>
</tr>
<tr>
<td>$2^{23}-1$</td>
<td>23</td>
<td>$x^{23}\cdot x^{18}+1$</td>
<td>8388607</td>
</tr>
<tr>
<td>$2^{23p}-1$</td>
<td>23</td>
<td>$x^{23}\cdot x^{21}\cdot x^{19}\cdot x^{16}\cdot x^7\cdot x^2+1$</td>
<td>8388607</td>
</tr>
<tr>
<td>$2^{31}-1$</td>
<td>31</td>
<td>$x^{31}\cdot x^{28}+1$</td>
<td>2147483647</td>
</tr>
<tr>
<td>$2^{33}-1$</td>
<td>33</td>
<td>$x^{33}\cdot x^{20}+1$</td>
<td>8589934591</td>
</tr>
<tr>
<td>$2^{35}-1$</td>
<td>35</td>
<td>$x^{35}\cdot x^{33}+1$</td>
<td>34359738367</td>
</tr>
<tr>
<td>$2^{39}-1$</td>
<td>39</td>
<td>$x^{39}\cdot x^{35}+1$</td>
<td>54975813887</td>
</tr>
<tr>
<td>$2^{41}-1$</td>
<td>41</td>
<td>$x^{41}\cdot x^{38}+1$</td>
<td>2199023255551</td>
</tr>
<tr>
<td>$2^{45}-1$</td>
<td>45</td>
<td>$x^{45}\cdot x^{44}\cdot x^{42}\cdot x^{41}+1$</td>
<td>35184372088331</td>
</tr>
<tr>
<td>$2^{47}-1$</td>
<td>47</td>
<td>$x^{47}\cdot x^{42}+1$</td>
<td>140737488355327</td>
</tr>
<tr>
<td>$2^{49}-1$</td>
<td>49</td>
<td>$x^{49}\cdot x^{40}+1$</td>
<td>562949953421311</td>
</tr>
<tr>
<td>$2^{51}-1$</td>
<td>51</td>
<td>$x^{51}\cdot x^{40}\cdot x^{48}+x^{45}+1$</td>
<td>2251799813685247</td>
</tr>
</tbody>
</table>
The following tables shows the PRBS polynomial for M8195A/M8196A that is used to generate the selected PRBS $2^n$-1.

Table 52  PRBS polynomials for AWG (M8195A/M8196A)

<table>
<thead>
<tr>
<th>PRBS</th>
<th>Shift Register Length</th>
<th>Polynomial</th>
<th>PRBS Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2^7$-1</td>
<td>7</td>
<td>$x^2+x^6+1$</td>
<td>127</td>
</tr>
<tr>
<td>$2^9$-1</td>
<td>9</td>
<td>$x^9+x^5+1$</td>
<td>511</td>
</tr>
<tr>
<td>$2^{11}$-1</td>
<td>11</td>
<td>$x^{11}+x^9+1$</td>
<td>2047</td>
</tr>
<tr>
<td>$2^{13}$-1</td>
<td>13</td>
<td>$x^{13}+x^{12}+x^2+x^1+1$</td>
<td>8191</td>
</tr>
<tr>
<td>$2^{15}$-1</td>
<td>15</td>
<td>$x^{15}+x^{14}+1$</td>
<td>32767</td>
</tr>
</tbody>
</table>

- For block type as **Static**, you need to specify the **Single Value** and the **Compare** feature.
- If you select **Block Type** as **Memory Pattern**, a **Select Pattern** window will open which allows you to load the memory patterns.
- For block type as **Link Training**, you need to specify the **Direction**.
- Click **Select Location Specific Patterns**. This opens with a drop-down selection where you can specify the ports or locations of specific patterns.
Setting up Patterns

- Select the ports or locations and then click **Select**. The settings option for each port or location will be added to the **Block Data** functional block.
- Click **Clear** if you want to remove port or location specific patterns and use single pattern for the block.

**Compare Feature**

The **Compare** feature allows you to compare the block data for a particular sequence. It provides you the freedom to modify the sequence without deleting the blocks.

**When to use/not use this feature**

Suppose you created a sequence with multiple blocks. Now, if you want to exclude particular block(s) from that sequence while comparing, instead of deleting the whole sequence, just set the compare functionality “OFF” which in-turn will disable that particular block(s) from the sequence for comparison.

**Block Settings**

The **Block Settings** section allows you to:
- Click on the corresponding ON/OFF toggle button to turn on the following features:
  - CDR
  - Error Insertion
• Click on the ON/OFF toggle button to enable the block settings on the sequence.
• Click on the ON/OFF toggle button to turn on the **Symbol Align** feature.
• Select disparity whether positive, negative or unchanged.
• Click on the ON/OFF toggle button to turn on the **Sync and Loop** feature.

**NOTE**
The Sync feature will be automatically turned on once you turn on the Sync and Loop feature.

• Use the drop down option to specify whether you want to apply trigger on either **Pulse** or **Pulse or PRBS Match**.

**NOTE**
The changes made in the **Block Settings** section are reflected on the selected block.

---

**Block Branches**

The **Block Branches** are used to add the branches within the sequence. You can add up to two branches in a sequence.

To add a **Block Branches**, click on the **Add Branch** button. The **Block Branches** section will appear as shown in the following figure:
The **Block Branches** section provides the following settings:

- **Source**: Use the drop-down list to specify the source for the branch.
- **Event**: Specify the event for the branch.
- **Go to Block**: Specify the block name to jump.
- **Enabled**: Use the ON/OFF toggle button to enable the branching option.
- **Click Add Branch** if you want to add another branch. Up to two branches can be added within the same block.
- **Click Delete** icon to delete the branch.

Once the branching is enabled in a block, the **Block Branches** icon will appear on the sequence block as shown in the following figure:

```
1. Sync and Loop  Length: 1  
  Clock Divider: 2
```

### Block Controls

The **Block Controls** section allows you to provide sink value at Ctrl Out A and Sys Out A/B. These values help you to trigger the given sink at different values that are defined i.e. Low, High or Pulse. Press **Add Control** to add more block controls. You can add up to four block controls.
Editing a Pattern in a Sequence Editor

The **Sequence Editor** user interface contains **Pattern Edit Pane** that allows you to edit the memory patterns.

Make sure to enable the **Show Patterns** option by clicking on the **Show Pattern** icon, present on the toolbar. This will display the **Pattern Edit Pane**, in case it is not visible in the **Sequence Editor**.

To edit a pattern, you have to first load it in the sequence block. To do so:

1. Select the block on which the patterns are loaded.
2. Go to **Sequence Setting** window and then select **Block Data** functional block.
3. Select the **Block Type** as **Memory Patterns**. A **Select Pattern** window will open which allows you to load the memory patterns. You can download large memory patterns (up to 2 Gb) on each channel.
4. Select the desired pattern and click **Select**.
5. The pattern will be loaded into the selected block as well as on the **Pattern Edit Pane**. See the following figure:

   ![Pattern Edit Pane](image)

6. Edit the patterns as explained in the section **Pattern Edit Pane** on page 444.
Sharing Sequences

The M8070B software currently does not allow the functionality to share the sequences. However, there is a workaround to share sequences.

Follow the given steps:

1. Go to File > and click Save Instrument State... Once you save the instrument state, the sequence settings are also saved in the Settings folder which is created at the following path: “Documents\Keysight\M8070B\Workspaces\Default\User\Settings”

2. Share Settings folder.

3. Copy the Settings folder at the same path on another system.

4. Go to File > and click Recall Instrument State.... The sequences will now appear in the Sequence Editor.
User-Defined Sequences

This section describes the basics of user-defined sequences.

A sequence is created and maintained by means of the Sequence Editor. A sequence consists of up to 500 blocks that can be looped. Each block can generate a pause signal (constant 0 or 1), a divided clock signal, a $2^n - 1$ PRBS, or a user pattern.

Single or multiple blocks can be looped. The sum of the blocks and the counted loops must not exceed 500. An overall loop restarts the sequence after it has come to its end.

Sequence Block Display

A new sequence consists of one block that is infinitely repeated (looped). By default, this block has a length of 512 bits and generates a Pause 0 signal (a continuous stream of zeros). All this is shown on the display.

Sequence Block Parameters

The **Sequence Setting** window allows you to change the contents and the trigger generation of a sequence block.

Choices are:

- **Block No.**: Can be up to 500 blocks.
- **Length**: This is the length of the pattern in bits for a standard pattern of 128 bits.
- **Block Type**: Clock, PRBS, Pulse, Static or Memory Patterns.
- **PRBS**: You can choose a PRBS of polynomial $2^n - 1$. The range of $n$ is 7, 10, 11, 15, 23, or 31. You can change the block length, if desired.
- **Divided Clock**: You can use this option to generate the signal at every nth clock pulse.
- **Memory Pattern**: When you select pattern type as memory pattern, a **Select Pattern** dialog will appear. You have to locate the pattern file and then click **OK**. The patterns will be loaded in the sequence.
Select Pattern Dialog

The **Select Pattern** dialog allows you to either select a single pattern for all the analyzer and Generator locations or setup individual patterns for selected locations.

**NOTE**

This operation will download the new sequences. If the **Sequence Editor** is already opened, then changes made in the **Sequence Editor** will not be saved.

This dialog provides the following tabs:

**All Locations**

This tab allows you to select a single pattern and download it to all locations.
You to select the pattern from the following options:

- **Clock**
- **Pulse**
- **PRBS**
  - Refer to the Table 51 on page -412 and Table 52 on page -413 for the list of available PRBS polynomials.
- **Static** - The 1/0 values describe the logic bit content and high/low values relate to the level. Select 0 or Low for low level patterns and 1 or High for high level patterns. If you select the pattern as “inverted”, then the value 1 can become low level and 0 can become the high level.
- **Memory**
  - In case the Memory option is selected, a Select Memory Pattern... button will appear.

When you click this button, the Select Pattern dialog will appear.
Selected Locations

This tab allows you to setup individual patterns for selected locations. You need to select the pattern from the following options:

- Clock
- Pulse
- PRBS
  
  Refer to the Table 51 on page -412 and Table 52 on page -413 for the list of available PRBS polynomials.

- Static
- Memory

In case the Memory option is selected, a Select Pattern dialog will appear to load the memory pattern.

If you wish to open the Sequence Editor with the selected patterns, either select the "Open sequence editor after applying changes" check-box or click the Sequence Editor... button.

Click Apply to apply the changes.
Setting up Patterns

Application Specific Patterns

This section describes how to select the patterns for a specific standards. These patterns are applicable for M8045A and AWG (M8195A/M8196A) modules.

OIF CEI

OIF CEI QPRBS13-CEI

This pattern is defined in CEI 56G-VSR-PAM4 appendix 16.C.3.1.

1. Select PRBS13-1 from hardware PRBS generator or use the factory pattern available at the following location:
   Factory\CEI\PRBS13Q-CEI_bit
2. Choose Line Coding as PAM4.
3. Set Symbol Mapping to Gray Coded (Default).

OIF CEI QPRBS31-CEI

This pattern is defined in CEI 56G-VSR-PAM4 appendix 16.C.3.2.

1. Select PRBS31-1 from hardware PRBS generator.
2. Choose Line Coding as PAM4.
3. Set Symbol Mapping to Gray Coded (Default).

IEEE 802.3

IEEE 802.3 QPRBS13

This pattern is defined in IEEE 802.3 clause 94.2.9.3. It is stored in a way that will output the correct PAM4 symbols when Symbol Mapping is set to Gray Coded.

1. Select the factory pattern available at the following location:
   Factory\IEEE\QPRBS13_Lane0_bit_SelectGrayCoded
2. Choose Line Coding as PAM4.
3. Set Symbol Mapping to Gray Coded (Default).
**IEEE 802.3 PRBS13Q**

This pattern is defined in IEEE 802.3 clause 120.5.11.2.3.

1. Select PRBS13-1 from hardware PRBS generator or use the factory pattern available at the following location:
   - Factory\IEEE\PRBS13Q_Lane0_bit
2. Choose Line Coding as PAM4.
3. Set Symbol Mapping to Gray Coded (Default).

For convenience additional lane 1 to lane 3 versions are stored at:
- Factory\IEEE\PRBS13Q_Lane1_bit
- Factory\IEEE\PRBS13Q_Lane2_bit
- Factory\IEEE\PRBS13Q_Lane3_bit

These additional versions are intended for multi-lane applications and using alternative seeds as defined in table IEEE 802.3 94–11.

**IEEE 802.3 PRBS31Q**

This pattern is defined in IEEE 802.3 clause 120.5.11.2.4.

1. Select PRBS31-1 from hardware PRBS generator.
2. In the block settings activate the Invert feature of the hardware PRBS generator.
3. Choose Line Coding as PAM4.
4. Set Symbol Mapping to Gray Coded (Default).

**IEEE 802.3 SSPRQ**

The IEEE/SSPRQ_bit_SelectGrayCoded (120.5.11.2.3) pattern corresponds to the pattern as defined in release 1.0 of the spec while IEEE/SSPRQ_bit_SelectGrayCoded_D1p5 (120.5.11.2.5) pattern is the version from Draft 1.5 of the spec. It is stored in a way that will output the correct PAM4 symbols when Symbol Mapping is set to Gray Coded.

1. Select the factory patterns available at the following location:
   - Factory\IEEE\SSPRQ_bit_SelectGrayCoded
   - Factory\IEEE\SSPRQ_bit_SelectGrayCoded_D1p5
2. Choose Line Coding as PAM4.
3. Set Symbol Mapping to Gray Coded (Default).
Pattern Editor

The pattern editor provides an interactive user-interface for creating, editing and importing the patterns.

How to Launch Pattern Editor

To launch the Pattern Editor:

- Go to the Menu Bar > Patterns and then select Pattern Editor.

The Pattern Editor will appear as shown in the following figure:

![Pattern Editor Interface](image)

The Pattern Editor user interface includes the following elements:

- Toolbar
- Settings Window
- Pattern Edit Pane
Setting up Patterns

Toolbar

The toolbar provides the following convenient pattern editing functions:

Table 53

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>New</td>
<td></td>
<td>Click this icon to create a new pattern. For details, refer to Creating New Patterns on page 428.</td>
</tr>
<tr>
<td>Open</td>
<td></td>
<td>Click this icon to open a pattern from a file. For details, refer to Opening Existing Patterns on page 431.</td>
</tr>
<tr>
<td>Save</td>
<td></td>
<td>Click this icon to save the current pattern. For details, refer to Saving Patterns on page 433.</td>
</tr>
<tr>
<td>Save As</td>
<td></td>
<td>Click this icon to change the properties of current pattern and then save it under different name. For details, refer to Saving Patterns on page 433.</td>
</tr>
<tr>
<td>Import</td>
<td></td>
<td>Click this icon to import patterns, edit them and use them for testing and analysis. For details, refer to Importing Patterns on page 436.</td>
</tr>
<tr>
<td>Export</td>
<td></td>
<td>Click this icon to export patterns in the desired location. These patterns can be used by other instruments for testing and analysis. For details, refer to Exporting Patterns on page 438.</td>
</tr>
<tr>
<td>Download</td>
<td></td>
<td>Click this icon to download the pattern to either all locations or on the selected locations. An orange icon indicates that the pattern is modified and is not yet downloaded to any location(s).</td>
</tr>
</tbody>
</table>
Copy These functions follow Microsoft Windows copy/paste functionality. You can perform the copy/paste operations in the following ways:
- Click on Copy/Paste icons
- Use keyboard shortcuts (Ctrl+C, Ctrl+V)
- Right click and use the context menu options

The Copy/Paste function allows you to:
- Select either the partial data or the complete symbols in a pattern and copy/paste it anywhere in the pattern.
- Use the copy/paste operations for the partial data across multiple instances of Pattern Editor, irrespective of the pattern coding.
- Use the paste operation to and from clipboard to Pattern Editor.

Please note that the paste operations for the complete pattern symbol is only allowed in the same pattern symbol coding.
This icon is only available when the partial data is copied from the pattern. Whenever a paste operation is done using this function, the underline data will be pasted.

Paste as String

Paste as Data

Undo Reverses the last editing action, such as typing, modifying or deleting text. When you do such actions, you can use the Undo command to restore them.
Keyboard shortcut - Ctrl + Z

Redo Restores the last editing action, such as typing, modifying or deleting text if no other actions have occurred since the last Undo.
Keyboard shortcut - Ctrl + R

Find Click this icon to open the Find Symbol dialog box and perform the search operation for a specified segment in the pattern. For details, see Find Symbol Dialog Box on page 439.

Select All Click this icon to select all the symbols in the pattern.
Keyboard shortcut - Ctrl + A

Block Edit Click this icon to perform block edit operations on currently selected pattern. For details, refer to Block Edit Operations on page 440.

Go To Click this icon if you want to jump to an arbitrary bit position. See Go To Bit Dialog Box on page 441.
The **Pattern Editor** allows you to perform following tasks on patterns:

- Create a new patterns. For details, refer to Creating New Patterns on page 428.
- Open and already existing patterns. For details, refer to Opening Existing Patterns on page 431.
- Save a patterns. For details, refer to Saving Patterns on page 433.
- Import supported patterns. For details, refer to Importing Patterns on page 436.
- Perform block edit operations. For details, refer to Interactive Link Training on page 466.
- Edit a patterns on Pattern Edit Pane. For details, refer to Pattern Edit Pane on page 444.

### Creating New Patterns

To create a new pattern:

1. Click the **New** icon present on the tool bar. This opens with the Create New Pattern sliding window as shown in the following figure:

2. Select the coding type. The **Pattern Editor** currently supports the following types of coding:
   - Bit (Binary)
   - 8B/10B
   - 128B/130B
   - 128B/132B
3 Specify the number of symbols. Use the UP and DOWN button to increase or decrease the number of symbols.

4 Specify the fill patterns.

5 Specify by using the ON/OFF toggle switch whether you want to use Mask and Squelch (Electric Idle). In Squelch, the amplifier output is zero.

6 After you have entered these parameters, click Create. The newly created pattern will appear in the Pattern Editor pane.

7 Click the Save icon to save the pattern. For more details, refer to Saving Patterns on page 433.

Downloading Patterns

You can also download the pattern to either selected locations or on all locations using the Download Pattern dialog. To do so, follow the given steps:

1 Create a new pattern or open an existing pattern.

2 Click on the Download button . If the pattern is not saved, a message will appear to save the pattern before downloading.

3 Once saved, a Download Pattern dialog will appear. This dialog allows you to download the selected pattern to either on all locations or on the selected locations.
Setting up Patterns

This dialog provides the following tabs:

- **All locations** - Use this tab to download the memory pattern on all locations. Since, it is a memory pattern, this dialog disable all other pattern options. Only, the memory pattern option is available.

- **Selected Locations** - Use this tab to download the current pattern to the selected locations. On selecting the check-box, the name of the current pattern will appear.
4 Click OK to download the pattern.

5 If you wish to open the Sequence Editor with the selected patterns, either select the "Open sequence editor after applying changes" check-box or click the Sequence Editor... button and then click OK.

Opening Existing Patterns

To open an existing user pattern:

1 Click the Open icon present on the tool bar.

   This opens the Open Pattern dialog, where you can locate and open the desired pattern. You can even perform the operations such as renaming and deleting the pattern file and creating new folders.
You can select the pattern from the following default folders:

1. **Shared**: Patterns that are shared between settings.
2. **Current**: Patterns that are local to current setting.
3. **Factory**: Factory supplied standard patterns. These patterns are read only and cannot be modified.

2. Click **Open** to load the patterns.
3. To rename a file, select the file and click **Rename**. The filename will become editable.
4. To delete a file, select the file and click **Delete**.
5. To add new folder, select location you want to create your folder and then click **New Folder**.
6. To rename a folder, select the folder and click **Rename**. The folder name will become editable.
7. To delete a folder, select the folder and click **Delete**.
Saving Patterns

To save the current user pattern:

1. Click the **Save** icon present on the tool bar. A **Save Pattern** dialog will appear which allows you to save the patterns under the defined file name and location.

You can use the **Save Pattern** dialog to perform the operations such as renaming and deleting the patterns. You can even create a new folder or save the patterns in the **Current** or **Shared** folders. The current folder is for current users while the shared folder is accessible by all users. If the pattern has already been saved earlier, the saved file will be updated.
2 Click on the Save As icon if you wish to change the properties of current pattern and then save it under different name. The current pattern can be either a non-captured pattern or a captured pattern.

a For saving a non-captured pattern, a Select Pattern Properties dialog will appear. This dialog provides the following options:

- Make a copy of current pattern with no change in pattern properties.
- Change the properties of current pattern. Using this option, you can change the pattern coding and enable/disable Squelch and Mask.
- You can save the entire pattern or can also provide the pattern range to be saved.

b For saving a captured pattern, a Select Captured Pattern Properties dialog will appear. This dialog provides the following options:
• Change the properties of current pattern. Using this option, you can change the pattern coding and enable/disable Mask, Squelch and Error as Mask.

The Use Error As Mask option is only visible when the Use Mask option is enabled and coding is same as captured pattern.

• Change the properties of current captured pattern. Using this option, you can change the pattern coding and enable/disable Mask, Squelch and Error as Mask.

• You can save the entire captured pattern or can also provide the pattern range to be saved.

• Click Override to remove all errors from the pattern.

3 Press Save As... button. A standard Save As Pattern dialog box will appear.
Importing Patterns

The M8070B Pattern Editor allows you to import patterns, edit them and use it for testing and analysis.

To import a pattern:

1. Click the `Import` icon. This opens the Select File dialog which allows you to locate the pattern. You are allowed to import patterns with any file extension (.ptrn and .txt).
2. Select the pattern and click Open in the Select File dialog.
3. If you import a .ptrn file, skip the step 4 and go to step 5.
4. However, if you import a .txt file, a Select Import Pattern Properties dialog will appear:
This dialog allows you to change the pattern coding and enable Squelch and Mask in the pattern.

5 Click **OK**. An **Import Pattern** dialog will appear as shown in the following figure:

![Import Pattern Dialog](image1)

6 Choose a location (shared or current) to save the pattern. You can also create a new folder.

7 Provide a file name and click **Import**. The imported patterns will appear in the **Pattern Edit Pane**.
Exporting Patterns

The M8070B Pattern Editor allows you to export patterns and use it for testing and analysis.

To export a pattern:

1. Click the Export icon. This opens the Select Pattern to Export dialog as shown in the following figure:

![Select Pattern to Export dialog](image)

2. Select the pattern and click Export. This opens the Export Pattern dialog.
3 Locate the path and file name for the .prtn file.
4 Click **Save** to export the data to the specified destination.

**Sharing Patterns**

You can share patterns to other users by exporting the pattern to a shared location and later importing that pattern to Pattern Editor. For details on how to export and import patterns, refer to [Exporting Patterns](#) on page 438 and [Importing Patterns](#) on page 436.

**Find Symbol Dialog Box**

The **Find Symbol** dialog box allows you to search for a specified bit sequence or symbols in the pattern. If you click **Find Next**, the next occurrence of this bit sequence or symbol is highlighted.
The search pattern can be entered in binary/hex/symbol format, depending on currently selected mode in pattern editor. You can continue editing the pattern while this dialog box is still open.

**Block Edit Operations**

The **Block Edit** window provides an easy way to modify parts of the pattern or the entire pattern at once. This can be used when setting up a new pattern. It can also be used as an optional technique for editing existing patterns.

Click on the **Block Edit** icon present on the toolbar. The **Block Edit** sliding window will appear as shown in the following figure:

![Block Edit Window](image)

With the **Block Edit** window, you can use the drop-down list to specify whether the block edit operation has to be performed on data or listed attributes. You can also define the range that is to be modified. The available options for the range are:

- **All**
  Choose this option to edit the entire pattern.

- **Range**
  Choose this option to select the range of bits, symbols or blocks entered in the **From** and **To** fields.

The **Block Edit** window contains the following tabs:

- **Fill**
  This tab allows filling the given range in the pattern with the specified value. The available options for the **Fill** tab are:
    - **Fill Pattern**
Fills the specified value to the given range in the pattern. You can only enter the patterns depending upon the pattern mode (Bit coded or Symbol coded) selected from Data View Mode.

- **Invert**
  Invert the bits. 0 becomes 1 and 1 becomes 0.

- **Rotate**
  This tab provides the following options:
  - **Rotate Symbol Left by:**
    Treats the pattern data in the specified range as a circular buffer and rotates the bits to the left by the specified amount. No data will be lost and what is at the start of the buffer will be at the end of the buffer after the rotation.
  - **Rotate Symbol Right by:**
    Treats the pattern data in the specified range as a circular buffer and rotates the bits to the right by the specified amount. No data will be lost and what is at the end of the buffer will be at the start of the buffer after the rotation.
  - **Align to Sequence:**
    Aligns the pattern data in the specified range to a specified pattern sequence.

**Go To Bit Dialog Box**

The **Go To** dialog box allows you to set the cursor to an arbitrary position in the pattern.

![Go To Symbol: (0-15)](image)

Enter the bit position (=address) or alternatively you can use the UP and DOWN arrow buttons to enter the bit position and then click OK. The cursor will be placed in front of the character with the selected bit.
Settings Window

The **Settings Window** allows you to set the visualizations of the currently selected patterns. This helps you to easily identify the data and attributes in the pattern.

The **Settings Window** provides the following options:

**Data View**

The **Data View** option allows you to set the following:

- **Data View Mode** - Select the data view mode as Bin, Hex, PAM4 No Coding, PAM4 Gray Coding and PAM4 Custom coding.
- **Show High Low** - Toggle the ON/OFF switch to display either high or low transition in the patterns. This option is only available in Bit coding.
- **Custom Symbol Mapping** - It appears only when you view the bit pattern as PAM4 Custom. It allows you to map the consecutive data bits to PAM4 symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10).
- **Show Continuous Stream** - Toggle the ON/OFF toggle switch to show continuous stream in the patterns. This option is only available in Bit coding.
- **Symbols Per Row** - Specify a number to view the specified number of symbols in each row.

![Settings Window Image]

**Colors**

The **Colors** option allows you to set the following:

- **Background Color** - Changes the background color of the pattern editor pane.
- **Caret Color** - Changes the color of the carat in the pattern.
- **Zero Color** - Changes the color of all occurrences of zeros (0) in the pattern.
Setting up Patterns

- **One Color** - Changes the color of all occurrences of ones (1) in the pattern.
- **Transition Color** - Changes the transition color in the pattern.
- **Mask Color** - Changes the color of the bits that are masked.
- **Squelch Color** - Changes the color of the bits that are squelch.
- **Attribute 1 Color** - Changes the color of attribute 1.
- **Attribute 0 Color** - Changes the color of attribute 0.

You can at anytime reset the color settings to default colors by pressing the **Reset to Default Colors** button.

---

**Visuals**

The **Visual** option allows you to set the following:

- **Data** - Changes the data appearance as selected from the data visual options.
- **Attributes** - Changes the attribute appearance as selected from the attributes visual options.
Pattern Edit Pane

The pattern edit pane displays the pattern and also allows you to edit it.

The pattern edit pane shows the symbol and data. You can edit selected data using the keyboard keys. Remember, the pattern edit pane does not allow you to enter any wrong data.

The pattern edit pane allows you to import and export patterns. For details on how to import and export the patterns, refer to Importing Patterns on page 436 and Exporting Patterns on page 438.

The pattern edit pane also allows you to save the current pattern with other pattern coding. You can right click on the pattern edit pane and use the context menu option (Save As) to save the current pattern or save the selected range of pattern. For details, refer Saving Patterns on page 433.

The pattern edit pane also allows the copy/paste functionality. Once you select the symbols in a pattern, you can copy them and paste it anywhere in the pattern. You can perform the copy/paste operations in the following ways:

- Click on Copy/Paste icons
- Use keyboard shortcuts (Ctrl+C, Ctrl+V)
- Right click and use the context menu options
Please note that the copy operation only allows a complete symbol to be copied.

It is possible to use the copy/paste operations across multiple instances of Pattern Editor window with same pattern coding.

The pattern edit pane also allows the undo and redo operations. Using this operation you can reverse or restore the last performed action. You can use the keyboard shortcuts (Ctrl+Z) for Undo and (Ctrl+R) for Redo operations.

The pattern edit pane also provides the scrolling feature which can be utilized using the keyboard and mouse. With a keyboard, you can use the up or down arrow keys to move the scrollbar. With a mouse, you can move scroll bar by clicking the scroll arrow at either end of the scroll bars, click empty portions of the scroll bar, or click and drag the scroll box. When you press the scroll bar using the mouse, a tool-tip appears which displays the current position of the symbol number.

Patterns consist of a sequence of symbols. A symbol can have the following type of coding:

1. Bit (Binary)
2. 8B/10B
3. 128B/130B
4. 128B/132B

The following figure shows the Pattern Edit Pane with a bit coded pattern (Binary) pattern:
The bottom of the Pattern Editor Pane indicates the position of the selected symbols and buttons to edit them. These buttons are only available when you create a pattern in bit coding and the data view mode is binary (BIN). You can use these buttons to:

- **0** - Set data 0
- **1** - Set data 1.
- **X** - Click this toggle button to add/remove mask on a data.
- **S** - Click this toggle button to add/remove squelch on a data.

You can use the buttons as well as the keyboard keys to move the pointer position to the left, right, up and down in the pattern.

In binary mode, when you click on any symbol, its position is displayed as following:

- The top of the Pattern Editor Pane displays the index of cursor (symbol) in current row.
- The bottom of the Pattern Editor Pane displays the symbol number.

The following figure shows the Pattern Editor Pane with a symbol coded (8B/10B) coded pattern:
You can use the **Settings Window** to enhance the visualizations of the current pattern. For details, refer to “Settings Window” on page -442.

**Symbol Attributes**

A symbol can have additional attributes to modify behavior. They are supported by all symbols. These are:

1. **Mask**: This attribute only affects the **Data In** ports. It specifies if the symbol is actually compared or masked (excluded from compare).

2. **Squelch**: This attribute only affect the **Data Out** ports. If this attribute is 1, a squelch (out of band) level is used.

In addition there are coding specific attributes, to control aspects of the coding like bypassing or using a scrambler.

**Editing a Pattern**

To edit a pattern:

1. Open an already existing pattern. Refer to Opening Existing Patterns on page 431.

2. If no pattern is available, a new pattern can be created. Refer to Creating New Patterns on page 428.

3. Select the bits to be edited in the patterns.

4. Use the keyboard to enter the required bits. It can be in form of 0 or 1.
5 If the current pattern is in use in some other location(s), then the orange Download button will get highlighted when the pattern is modified.

6 Click on the Download button to download the pattern. Once it is download, the green Download button will appear.

Editing a Captured Pattern

To edit a captured pattern, it needs to be converted to an editable pattern. Follow the given steps make the captured pattern editable:

1 Open an already saved captured pattern. Refer to Opening Existing Patterns on page 431.

2 Select the bits to be edited in the patterns

3 Use the keyboard to enter the required bits. It can be in form of 0 or 1.

A Select Captured Properties dialog will appear:

4 Change the properties of current pattern. Using this option, you can change the pattern coding and enable/disable Mask, Squelch and Error as Mask.

The Use Error As Mask option is only visible when the Use Mask option is enabled and coding is same as captured pattern.

5 Click Override to remove all errors from the pattern.

6 Click Save As. A Save Pattern As dialog will appear.

7 Specify the name and location and click Save.
Bit Coding

The following figure shows the pattern edit pane with a bit coded pattern in binary (BIN) mode:

The bottom of the pattern edit pane indicates the position of the selected symbols and buttons to edit them. These buttons are only available when you create a pattern in bit coding and the data view mode is binary (BIN). You can use these buttons to:

0 - Set data 0
1 - Set data 1.
X - Click this toggle button to add/remove mask on a data.
S - Click this toggle button to add/remove squelch on a data.

You can use the <A> buttons as well as the keyboard keys to move the pointer position to the left, right, up and down in the pattern.

The bottom of the pattern edit pane also displays the symbol number which indicates the number.

You can use the Settings Window to enhance the visualizations of the current pattern. For details, refer to “Settings Window” on page 442.

To encode a bit coded symbol 1, 2 or 3 bits are needed. This depends on the use of mask and squelch:
## Setting up Patterns

Table 54  Plain bit coding without using mask or squelch

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Data</td>
<td>Data bit</td>
</tr>
</tbody>
</table>

Table 55  Mask is used

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Data</td>
<td>Data bit</td>
</tr>
<tr>
<td>1</td>
<td>Mask</td>
<td>Mask (ignored on DataOut)</td>
</tr>
</tbody>
</table>

Table 56  Squelch is used

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Data</td>
<td>Data bit</td>
</tr>
<tr>
<td>1</td>
<td>Squelch</td>
<td>Squelch (ignored on DataIn)</td>
</tr>
</tbody>
</table>

Table 57  Mask and Squelch are used

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Data</td>
<td>Data bit</td>
</tr>
<tr>
<td>1</td>
<td>Mask</td>
<td>Mask (ignored on DataOut)</td>
</tr>
<tr>
<td>2</td>
<td>Squelch</td>
<td>Squelch (ignored on DataIn)</td>
</tr>
</tbody>
</table>
8B/10B Coding

The following figure shows the pattern edit pane with a 8B/10B coded pattern:

You can use the Settings Window to enhance the visualizations of the current pattern. For details, refer to Settings Window on page 442.

This type of pattern contain:

- **Symbol**: 8B/10B coding have 8 bits in one symbol.
- **Attributes**: It has the following attributes:
  - **Mask**: This attribute only affects the Data In ports.
  - **Squelch**: This attribute only affects the Data Out ports.
  - **Scrambler Enable**: This attribute enables/disables the scrambler.
  - **Scrambler Pause**: This attribute is used to pause scrambler for some special symbol.
  - **Scrambler Reset**: This attribute is used to reset scrambler LFSR (Linear feedback shift register).
  - **Start of frame**: This attribute enables/disables the start of frame marker.
  - **K/D**: This attribute specifies whether the symbol bits are control characters or data.
  - **Data**: Specifies data bits.
To encode an 8B/10B symbol, 16 bits (2 bytes) are used:

**Table 58**

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Data</td>
<td>Symbol data</td>
</tr>
<tr>
<td>8</td>
<td>K/D</td>
<td>0 = D-character, 1 = K-character</td>
</tr>
<tr>
<td>9</td>
<td>Reserved for future use. Must be set to 0</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Mask</td>
<td>Mask (if present, ignored on DataOut)</td>
</tr>
<tr>
<td>11</td>
<td>Squelch</td>
<td>Squelch (if present, ignored on DataIn)</td>
</tr>
<tr>
<td>12</td>
<td>Enable Scrambler</td>
<td>Enable Scrambler (ignored on DataIn)</td>
</tr>
<tr>
<td>13</td>
<td>Pause Scrambler</td>
<td>Pause Scrambler (ignored on DataIn)</td>
</tr>
<tr>
<td>14</td>
<td>Reset Scrambler</td>
<td>Reset Scrambler (ignored on DataIn)</td>
</tr>
<tr>
<td>15</td>
<td>Start of Frame</td>
<td>Start of Frame (ignored on DataOut)</td>
</tr>
</tbody>
</table>
128B/130B Coding

The following figure shows the pattern edit pane with a 128B/130B coded pattern:

You can use the **Settings Window** to enhance the visualizations of the current pattern. For details, refer to **Settings Window** on page 442.

This type of pattern contain:

- **Symbol**: 128B/130B coding having 128 bit in one symbol.
- **Attributes**: It has the following attributes:
  - **Mask**: This attribute only affects the **Data In** ports.
  - **Squelch**: This attribute only affects the **Data Out** ports.
  - **Scrambler Enable**: This attribute enables/disables scrambler.
  - **Scrambler Pause**: This attribute is used to pause the scrambler for some special symbol.
  - **Scrambler Reset**: This attribute is used to reset the scrambler LFSR (Linear feedback shift register).
  - **Scrambler Bypass**: This attribute is used to bypass the scrambling over the symbol.
  - **Scrambler Bypass Byte 0**: If this bit is enabled, it does not allow scrambling over the symbol.
• **Do DC Balancing** - This attribute is used to set DC balancing over symbol.
• **Reset DC Balancing** - This attribute resets the DC balancing state.
• **Send Scrambled State** - This attribute specifies whether to send the scrambled state.
• **Reset Parity** - This attribute is used to reset the parity bit.
• **Pause Parity** - This attribute is used to pause the parity bit.
• **Start of frame** - This attribute enables/disables the start of frame marker.
• **Framing** - This attribute enables/disables the start of frame marker.
• **Data** - Specifies the data bits.

To encode a 128B/130B symbol, 144 bits (18 bytes) are used:

**Table 59**

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Framing</td>
<td>Framing bits</td>
</tr>
<tr>
<td>129:2</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>130</td>
<td>Mask</td>
<td>Mask (if present, ignored on DataOut)</td>
</tr>
<tr>
<td>131</td>
<td>Squelch</td>
<td>Squelch (if present, ignored on DataIn)</td>
</tr>
<tr>
<td>132</td>
<td>Reset Scrambler</td>
<td>Scrambler reset (ignored on DataIn)</td>
</tr>
<tr>
<td>133</td>
<td>Pause Scrambler</td>
<td>Scrambler pause (ignored on DataIn)</td>
</tr>
<tr>
<td>134</td>
<td>Bypass Scrambler</td>
<td>Scrambler bypass</td>
</tr>
<tr>
<td>135</td>
<td>Bypass Byte 0 Scrambler</td>
<td>Scrambler bypass byte 0</td>
</tr>
<tr>
<td>136</td>
<td>Do DC Balancing</td>
<td>Do DC balancing (ignored on DataIn)</td>
</tr>
<tr>
<td>137</td>
<td>Reset DC Balancing</td>
<td>Reset DC balancing (ignored on DataIn)</td>
</tr>
<tr>
<td>138</td>
<td>Send Scrambler State</td>
<td>Send scrambler state (ignored on DataIn)</td>
</tr>
<tr>
<td>139</td>
<td>Reset Parity</td>
<td>Reset Parity (ignored on DataIn)</td>
</tr>
</tbody>
</table>
### 128B/132B Coding

The following figure shows the pattern editor pane with a 128B/132B coded pattern:

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>140</td>
<td>Pause Parity</td>
<td>Pause Parity (ignored on DataIn)</td>
</tr>
<tr>
<td>141</td>
<td>Start of Frame</td>
<td>Start of Frame (ignored on DataOut)</td>
</tr>
<tr>
<td>143:142</td>
<td></td>
<td>Reserved for future use. Must be set to 0</td>
</tr>
</tbody>
</table>

**NOTE** When using 128/130 coding pattern contains Sync Symbols to achieve Symbol Alignment. These Sync Symbols need to be at least 16 symbols apart.
This type of pattern contains:

- **Symbol**: 128B/132B coding having 128 bit in one symbol.
- **Attributes**: It has the following attributes:
  - **Mask**: This attribute only affects the **Data In** ports.
  - **Squelch**: This attribute only affects the **Data Out** ports.
  - **Scrambler Reset**: This attribute is used to reset the scrambler LFSR (Linear feedback shift register).
  - **Scrambler Pause**: This attribute is used to pause the scrambler for some special symbol.
  - **Scrambler Bypass**: This attribute is used to bypass the scrambling over the symbol. If this bit is enabled, it will not allow scrambling over the symbol.
  - **Scrambler Bypass Byte 0**: If this bit is enabled, it does not allow scrambling over the symbol.
  - **Do DC Balancing**: This attribute is used to set DC balancing over the symbol.
  - **Reset DC Balancing**: This attribute resets the DC balancing state.
  - **Send Scrambled State**: This attribute specifies whether to send the scrambled state.
  - **Reset Parity**: This attribute is used to reset the parity bit.
  - **Pause Parity**: This attribute is used to pause the parity bit.
  - **Start of frame**: This attribute enables/disables the start of frame marker.
  - **Framing 0 1 2 3**: This attribute enables/disables the start of frame marker.
  - **Data**: Specifies the data bit.

You can edit selected data using the keyboard.

To encode a 128B/132B symbol, 144 bits (18 bytes) are used:

<table>
<thead>
<tr>
<th>Bit offset range</th>
<th>Bit (range) name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Framing</td>
<td>Framing bits</td>
</tr>
<tr>
<td>131:4</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>132</td>
<td>Mask</td>
<td>Mask (if present, ignored on DataOut)</td>
</tr>
<tr>
<td>133</td>
<td>Squelch</td>
<td>Squelch (if present, ignored on DataIn)</td>
</tr>
<tr>
<td>Bit offset range</td>
<td>Bit (range) name</td>
<td>Description</td>
</tr>
<tr>
<td>------------------</td>
<td>------------------------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>134</td>
<td>Reset Scrambler</td>
<td>Scrambler reset (ignored on DataIn)</td>
</tr>
<tr>
<td>135</td>
<td>Pause Scrambler</td>
<td>Scrambler pause (ignored on DataIn)</td>
</tr>
<tr>
<td>136</td>
<td>Bypass Scrambler</td>
<td>Scrambler bypass</td>
</tr>
<tr>
<td>137</td>
<td>Bypass Byte 0 Scrambler</td>
<td>Scrambler bypass byte 0</td>
</tr>
<tr>
<td>138</td>
<td>Do DC Balancing</td>
<td>Do DC balancing (ignored on DataIn)</td>
</tr>
<tr>
<td>139</td>
<td>Reset DC Balancing</td>
<td>Reset DC balancing (ignored on DataIn)</td>
</tr>
<tr>
<td>140</td>
<td>Send Scrambler State</td>
<td>Send scrambler state (ignored on DataIn)</td>
</tr>
<tr>
<td>141</td>
<td>Reset Parity</td>
<td>Reset Parity (ignored on DataIn)</td>
</tr>
<tr>
<td>142</td>
<td>Pause Parity</td>
<td>Pause Parity (ignored on DataIn)</td>
</tr>
<tr>
<td>143</td>
<td>Start of Frame</td>
<td>Start of Frame (ignored on DataOut)</td>
</tr>
</tbody>
</table>

**NOTE**

When using 128/132 coding pattern contains Sync Symbols to achieve Symbol Alignment. These Sync Symbols need to be at least 16 symbols apart.
Pattern Capture

The M8020A/M8030A/M8040A Analyzer captures the data received from the device under test. The captured data bits are displayed in the pattern capture pane in binary or 8b/10b symbol coding. The received data is compared with the expected data and the errored bits/symbols are highlighted. The captured data can be saved for post processing. The maximum capture memory for M8041A, M8051A, M8061A and M8045A is 2 Gb and for M8062A is 1 Gb. However, it also depends on the holdoff length which represents the amount of symbols in which the trigger events will be ignored.

How to Launch Pattern Capture Window

To launch the Pattern Capture window:
- Go to the Menu Bar > Patterns and then select Pattern Capture.

The Pattern Capture window will appear as shown in the following figure:

The Pattern Capture window includes the following elements:
- Toolbar
- Pattern Captured Pane
- Captured Results
- Parameters Window
Toolbar

The toolbar provides the following convenient pattern capture functions:

### Table 61

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Start</td>
<td>Starts capturing the current pattern</td>
</tr>
<tr>
<td></td>
<td>Stop</td>
<td>Stops capturing the current pattern</td>
</tr>
<tr>
<td></td>
<td>Reset</td>
<td>Resets the values of acquisition parameters</td>
</tr>
<tr>
<td></td>
<td>Manual Trigger</td>
<td>Manually starts the event that is triggering the capture logic.</td>
</tr>
<tr>
<td></td>
<td>Save Captured Data</td>
<td>Opens the “Save As” dialog which allows to save the captured data patterns as a separate pattern in the workspace (shared/current). Use this option to save the data and the error information. The data is saved as a sequence of one data bit and one error(compared) bit. This option enables you to save the captured pattern and view it later, along with the error information (errored bits). This option is applicable only when the ‘Capture Only’ parameter in the Pattern Capture measurement is set to OFF.</td>
</tr>
<tr>
<td></td>
<td>Save As</td>
<td>Click this icon to change the properties of current pattern and then save it under different name. For details, refer to Saving Patterns on page 433. Use this option to save only the captured data bits, without saving any errored bits information. Additionally, you can use this option to change the pattern properties, such as adding mask/squelch, saving in different encoding, and setting up the range.</td>
</tr>
<tr>
<td></td>
<td>Export</td>
<td>Click this icon to export patterns in the desired location. These patterns can be used by other instruments for testing and analysis. For details, refer to Exporting Patterns on page 438.</td>
</tr>
</tbody>
</table>
Parameters Window

The **Parameters** window have the following acquisition and show parameters for pattern capture.

**Acquisition Parameters**

- **Analyzer** - Use this drop-down menu to select the channel against which the data capture has to be performed.
- **Trigger** - Selects the event that is triggering the captured logic. It can be captured on the following four stop events:
  - **Immediately** - Starts capturing the data immediately and displays the captured data.
  - **Error** - Starts capturing the data when it receives an errored bit and displays the captured data.
  - **CTRL IN A** - Waits for a trigger signal from CTRL IN A port and displays the captured data.
• **CTRL IN B** - Waits for a trigger signal from CTRL IN B port and displays the captured data.

• **Slope** - Selects the edge (rising edge or falling edge) of CTRL IN A or CRL IN B that is triggering the captured logic.

• **Capture In Memory** - Enables you to capture and save the data into system’s memory and helps in performance optimization.
  - When the **Capture In Memory** toggle button is **On**, the system saves the data into the internal memory only.
  - When the **Capture In Memory** toggle button is **Off**, the system saves the data into the external hard drive.

• **Capture Only** - Enables you to capture data without comparison.
  - When the **Capture Only** toggle button is **On**, the system captures the data but does not compare to verify if the bit is errored or not.
  - When the **Capture Only** toggle button is **Off**, the system captures the default data.

• **Holdoff** - Defines the minimum of data bits to capture before the trigger event occurs. This value is adjusted to a multiple of the current symbol granularity.

• **Capture Depth** - Defines the minimum of data bits to capture including holdoff. This value is adjusted to a multiple of the current symbol granularity.

**Show Parameters**

• **View Coded Pattern As** - Displays the coded pattern (8B/10B) in Binary, Hex or Symbol view.

• **View Bit Pattern As** - Displays the captured bit coded pattern in Binary, Hex, PAM3, PAM4 No Coding, PAM4 Gray Coding and PAM4 Custom coding.

• **Symbols Per Row** - Displays the Symbols per row in Binary, Hex, PAM4-No Coding, PAM4-GRAY Coding, and PAM4-Custom view.

• **Custom Symbol Mapping** - It appears only when you view the bit pattern as PAM4 Custom. It allows you to map the consecutive data bits to PAM4 symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10).
How to Capture a Pattern

The following example explains the steps to capture a pattern to display errored bits.

1. Switch to Parameters window.
2. Set the acquisition parameters are shown below:
   - Location: M1.DataIn1
   - Trigger: Error
   - Holdoff: 500
   - Capture Depth: 10000
3. Click Start button. A message “Waiting for Trigger” will appear. You can click Manual Trigger to manually trigger the captured logic.
4. The captured data will be displayed in the Pattern Captured pane. The errored bits are marked red as shown in the following figure:
Pattern Capture Pane

The **Pattern Capture Pane** displays the captured pattern in the binary or 8b/10b symbol coding.

![Pattern Capture Pane](image)

The errored bits in the captured patterns are marked red. You can use the **Error Navigation** buttons to jump to next, previous, first or last error.

Please note that the **Pattern Capture** pane does not allow editing feature. This means you cannot edit the captured pattern. However, if you want to edit a captured pattern, you have to first save it and then open it in the **Pattern Editor**. For details on how to edit pattern, refer to **Editing a Pattern** on page 447. Using a **Pattern Editor**, you can also save the results in different encoding schemes.
Setting up Patterns

Saving a Captured Pattern

You can save the captured pattern for post processing. To do so;

- Click **Save** icon. This will open a **Save Captured Pattern** dialog.

- Specify the folder where it will be saved.
- Enter a file name and click **Save**. The current pattern will be saved under the filename.

You can open the saved file in the **Sequence Editor** and then download it to module to create a sequences. For details, refer to **Sequence Editor** on page 389.
Capture Results Pane

The **Capture Results** pane displays the results of the patterns captured.

![Capture Results Table]

The results are summarized as following:

- **Location** - Displays the location on which pattern capture is performed.
- **Capture Status** - Displays the current status of the capturing event as 'Finished', 'Stopped' or 'Waiting for Trigger'.
- **First Error** - Displays the position of first error bit.
- **Last Error** - Displays the position of last error bit.
- **Errors Count** - Displays the total number of errored bits.
- **Holdoff** - Displays the minimum number of data bits to capture before the trigger event occurs.
- **Capture Depth** - Displays the minimum number of data bits to capture including holdoff.
Interactive Link Training

PCI Express 3.0/4.0 Testing

Interactive link training is required for link equalization testing as outlined in the PCI Express (R) Architecture PHY Test Specification.

LTSSM (Link Training and Status State Machine)

Link Training and Status State Machine (LTSSM) is the sub-block that drives and controls the link initialization, and training process for a PCIe device to enable the normal data exchange between the two devices over the link. LTSSM operates at the physical layer level and exchanges physical layer packets (Ordered sets such as TS1 and TS2) to initialize, train, and manage the link.

Two PCIe 3.0/4.0 instruments exchange Training Sequences as shown in the following diagram:

LTSSM States

LTSSM transits through various states and sub-states during link initialization, training, and management. The entry and exit of each of these states and the exchange of packets (Ordered sets) between the two devices during each state is as per the PCIe specifications.

As per the PCIe specifications, LTSSM has 11 states and further sub-states. These states are referred to frequently in this chapter to describe LTSSM testing using the Keysight LTSSM Tester tool. Following is a list of these states followed by a diagram to illustrate the sequence of these states as per the PCIe specifications.

- Detect
- Quiet
- Polling
- Configuration
- L0
- Recovery

Training Sequences are also used to switch the link to low power states.
The following figure displays the top-level states of LTSSM.

The Link Training starts in state “Detect”. The purpose of this state is to detect when a far end termination is present. In the “Polling” state, bit lock and Symbol lock are established and Lane polarity is configured. In “Configuration”, both the Transmitter and Receiver are sending and receiving data at the negotiated data rate. In “Recovery”, both the Transmitter and Receiver are sending and receiving data using the
configured Link and Lane number as well as the previously supported data rate(s). An active link that can transport transaction layer packets is in state “L0”. All power management states are entered from this state.

The intent of the “Disabled” state is to allow a configured Link to be disabled until directed or Electrical Idle is exited (i.e., due to a hot removal and insertion) after entering “Disabled”. The “Loopback” is intended for test and fault isolation use.

**LTSSM Tests for PCIe 3.0/4.0**

You can execute the following types of LTSSM tests for PCIe 3.0/4.0:

**Table 62**

<table>
<thead>
<tr>
<th>Test Number</th>
<th>Test Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.3</td>
<td>Add-in Card Transmitter Initial Tx EQ Test for 8.0GT/s</td>
</tr>
<tr>
<td>2.4</td>
<td>Add-in Card Transmitter Link Equalization Response Test for 8GT/s</td>
</tr>
<tr>
<td>2.7</td>
<td>System Board Transmitter Link Equalization Response Test for 8GT/s</td>
</tr>
<tr>
<td>2.10</td>
<td>Add-in Card Receiver Link Equalization Test for 8GT/s</td>
</tr>
<tr>
<td>2.11</td>
<td>System Board Receiver Link Equalization Test for 8GT/s</td>
</tr>
</tbody>
</table>
Test Setup

The following block diagram shows the setup for test 2.3:

The following block diagram shows the setup for test 2.4:
The following block diagram shows the setup for test 2.7:

The following block diagram shows the setup for test 2.10:
The following block diagram shows the setup for test 2.11:

M8070B support for PCIe3.0/4.0 link training using M8020A

Refer the section Link Training Configuration on page 401 for the PCIe 3.0 and PCIe 4.0 parameters which are added to pattern sequence language for specifying certain values to configure the LTSSM.

Link Training Configuration

You can configure the link training parameters to control LTSSM using the Sequence Settings window. For details on link training parameters, refer to Link Training Configuration on page 401.

Test Procedure

Follow the given steps to perform link training for test 2.3:
1. In the M8070B software load the instrument state PCIe_PHY2.3_Test.
2. Power on the DUT.
3. Enable the Outputs of the M8041A.
4. Reset the DUT by pressing the reset button on the CBB.
5. With this setup everything is prepared for capturing the data for the P0 preset. Hit the Break button in the Sequence Editor to start the link training. If link training was successful the Status Indicator should show that the sequencer of the generator is executing block 4 or 5 and that there are no bit errors.
6 Set up the oscilloscope.
7 For shutting down the PCIe link hit the Break button again. The sequencer of the generator should return to block 2.
8 Before taking the measurement for P1 the test pattern has to be changed. For this select block 4 of the generator sequence. Under Sequence Settings > Block Data change the memory pattern to compliancePatternHeaderP1Lane0. This pattern can be found in the Current directory. Not changing the pattern will cause the SIG test software to show the wrong preset number, but won’t affect the test results otherwise.
9 Do the same for block 4 of the error detector sequence.
10 Under Sequence Settings > Instrument Configuration > Link Training PCIe (3.0 or 4.0) and change the DUT Initial Preset to P1.
11 Download the changed sequence.
12 Repeat the test as for P0 and then repeat the test procedure for P2 through P9.
13 Start the SIG software and load all captured files into the Preset Test.

Link Training Log

The Link Training Log window displays the log generated while initiating the link training test. All information regarding the executed tests and their status are displayed with the date and time stamp. This helps to identify the root cause of a problem. For instance, the Link Training Log shows test failure due to an unexpected LTSSM state change.

The following figure shows the log generated by the link training test for PCIe 3.0.
The following figure shows the log generated while initiating the link training test for PCIe 4.0:

You can open/close the Link Training Log window by clicking on the `Show/Hide Link Training Log` icon present in the status bar. The `Show/Hide Link Training Log` icon with orange background indicates an update or new entry in the link training log.

**User Calibrated Presets**

It specifies whether BERT’s Data Out should use user-calibrated presets or standard presets during link training. Turning it on means that BERT’s Data Out will use de-emphasis/pre-shoot values that had been previously calibrated, otherwise it will use standard de-emphasis/pre-shoot values defined by the PCIe specification (defined below). By default this option is turned off which means that standard presets will be used.

The following table shows standard preset from PCIe specification:

<table>
<thead>
<tr>
<th>Preset Number</th>
<th>De-emphasis (dB)</th>
<th>Preshoot (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0</td>
<td>-6.0</td>
<td>0.0</td>
</tr>
<tr>
<td>P1</td>
<td>-3.5</td>
<td>0.0</td>
</tr>
<tr>
<td>P2</td>
<td>-4.5</td>
<td>0.0</td>
</tr>
<tr>
<td>P3</td>
<td>-2.5</td>
<td>0.0</td>
</tr>
<tr>
<td>P4</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>P5</td>
<td>0.0</td>
<td>1.8</td>
</tr>
</tbody>
</table>
M8070B support for USB 3.0/3.1 link training using M8020A

The M8020A system allows you to test the physical layer compliance of a USB 3.0 (SuperSpeed) and USB 3.1 (SuperSpeedPlus) DUT. It provides the following types of testing:

- Transmitter Testing for USB 3.0/3.1
- Receiver Jitter Tolerance Testing for USB 3.0/3.1

The M8070B software provides the parameters which can be configured for link training USB 3.0 and USB 3.1.

LTSSM (Link Training and Status State Machine)

Link Training and Status State Machine (LTSSM) is the sub-block that drives and controls the link initialization, and training process for a USB device to enable the normal data exchange between the two devices over the link. LTSSM operates at the physical layer level and exchanges physical layer packets (Ordered sets such as TS1 and TS2) to initialize, train, and manage the link.

Two USB 3.0/3.1 instruments exchange Training Sequences as shown in the following diagram:

```
Device A  --TS--  Device B  --TS--

Training Sequences are also used to switch the link to low power states.
```
LTSSM States

LTSSM transits through various states and sub-states during link initialization, training, power management and error testing. The entry and exit of each of these states and the exchange of packets (Ordered sets) between the two devices during each state is as per the USB specifications.

LTSSM consist of 12 main link states and their sub-states. These states and sub-states are responsible for link initialization, training, power management and error testing.

The following figure displays the top-level states of LTSSM.
The USB 3.0 and 3.1 LTSSM consists following states and their sub-states:

1. **Rx.Detect** - Rx.Detect is the power on state of the LTSSM for both a downstream port and an upstream port. It is also the state for a downstream port upon issuing a Warm Reset, and the state for an upstream port upon detecting a Warm Reset from any other link state except eSS.Disabled. The purpose of Rx.Detect is to detect the impedance of far-end receiver termination to ground.

   It contains three sub-states:
   - **Rx.Detect.Reset** - Rx.Detect.Reset is a default reset state used by the two ports to synchronize the operation after a Warm Reset; this substate exits immediately if Warm Reset is not present.
   - **Rx.Detect.Active** - Rx.Detect.Active is a sub-state for far-end receiver termination detection.
   - **Rx.Detect.Quiet** - Rx.Detect.Quiet is a power saving sub-state in which the function of a far-end receiver termination detection is disabled. A port will perform the far-end receiver termination detection periodically during Rx.Detect.

2. **Polling** - Polling is a state for port capability negotiation and link training. During Polling, a Polling.LFPS handshake shall take place between the two ports to synchronize the operation after a Warm Reset; this substate exits immediately if Warm Reset is not present.

   It contains the following sub-states:
   - **Polling.LFPS** - Polling.LFPS is a substate designed to establish the PHY’s DC operating point, and to synchronize the operations between the two link partners after exiting from Rx.Detect. This is also a substate for a port to identify itself based on various Polling.LFPS signatures.
   - **Polling.LFPSPlus** - Polling.LFPSPlus is a substate where the port SuperSpeedPlus operation performs SCD2 handshake, for additional confirmation of the SuperSpeedPlus capability of its link partner.
   - **Polling.PortMatch** - Polling.PortMatch is a substate where the two ports in SuperSpeedPlus operation perform the LBPM handshake, for announcing, matching, and deciding the operation on the highest common capability between the two link partners.
- **Polling.PortConfig**: Polling.PortConfig is a substate where a port configures its PHY according to PHY Capability LBPM matched in Polling.PortMatch, and synchronizes with its link partner in exiting from this state to Polling.RxEQ. Depending on matched PHY Capability LBPM, a port may configure its PHY for SuperSpeed operation or SuperSpeedPlus operation.

- **Polling.RxEQ**: Polling.RxEQ is a substate for receiver equalization training. A port is required to complete its receiver equalization training.

- **Polling.Active**: Polling.Active is a substate that continues the link’s Enhanced SuperSpeed training.

- **Polling.Configuration**: Polling.Configuration is a substate where the two link partners complete the Enhanced SuperSpeed training.

- **Polling.Idle**: Polling.Idle is a substate where the port decodes the TS2 ordered set received in Polling.Configuration and determines the next state.

3. **U0**: U0 is the normal operational state where packets can be transmitted and received. U0 does not contain any substate machines.

4. **Recovery**: The Recovery link state is entered to retrain the link, or to perform Hot Reset, or to switch to Loopback mode. In order to retrain the link and also minimize the recovery latency, the two link partners do not train the receiver equalizers. Instead, the last trained equalizer configurations are maintained.
   It contains three sub-states:
   - **Recovery.Active**: Recovery.Active is a substate to train the Enhanced SuperSpeed link by transmitting the TS1 ordered sets.
   - **Recovery.Configuration**: Recovery.Configuration is a substate designed to allow the two link partners to achieve the Enhanced SuperSpeed handshake by exchanging the TS2 ordered sets.
   - **Recovery.Idle**: Recovery.Idle is a substate where a port decodes the link configuration field defined in the TS2 ordered set received during Recovery.Configuration and determines the next state.

5. **Loopback**: Loopback is intended for test and fault isolation. Loopback includes a bit error rate test (BERT) state machine. A loopback master is the port requesting loopback. A loopback slave is the port that retransmits the symbols received from the loopback master.
It contains two sub-states:

- **Loopback.Active** - Loopback.Active is a sub-state where the loopback test is active. The loopback master is sending data(commands) to its loopback slave. The loopback slave is either looping back the data or detecting/executing the commands it received from the loopback master.

- **Loopback.Exit** - Loopback.Exit is a sub-state where a loopback master has completed the loopback test and starts the exit from Loopback.

SuperSpeedPlus uses some additional LTSSM states to configure the 10G operation mode. LFPS handshake is divided into more states SCD1.LFPS, SCD2.LFPS (SuperSpeedPlus Capability Declaration) and LBPM (low power signaling mechanism for two SuperSpeedPlus ports to communicate with each other).

**Link Training Methods**

Following are the link training methods for USB 3.0 and USM 3.1:

- **WarmReset** (only for Devices – upstream ports)

  A WarmReset generated by downstream port to upstream port; done when ‘Device’ is selected. A WarmReset consists of a continuous LFPS (Low Frequency Periodic Signal).

**Loopback Training**

Loopback testing provides a standard way to quantify the bit error rate (BER) for established links between host and device. There is one loopback master and one loopback slave in the loopback configuration. The loopback master is the port that has the Loopback bit asserted in TS2 ordered sets. A loopback slave is the port that retransmits the symbols received from the loopback master. Master checks returned data for errors.

Loopback.Active is a sub-state where the loopback test is active. The loopback master is sending data(commands) to its loopback slave. The loopback slave is either looping back the data or detecting/executing the commands it received from the loopback master.

**Sequence**

For performing compliance tests the DUT has to be ‘trained’ into loopback mode. The pattern sequencer available in the M8070B software is able to set up a USB 3.x DUT into the specific loopback mode. The sequencer is also able to send compliance pattern to the DUT and can compare the received pattern with expected pattern for measuring e.g. bit error rates.
The pattern sequence language is based on XML. The pattern sequence language can be created and edited using the Sequence Editor in the M8070B software interface.

If symbol width 10 or 132 are selected following additional parameters will be visible on the right hand side in the Sequence Editor in the Parameter Window. On selecting the Symbol Width 10, the parameters for Link Training USB 3.0 are available in the Parameter Window. Similarly, on selecting the Symbol Width 132, the parameters for Link Training USB 3.1 are available in the Parameter Window.

Refer the section Link Training Configuration on page 401 for the parameters which are added to pattern sequence language for specifying certain values to configure the LTSSM.

The following figure shows an example of the link training sequence for USB 3.0 on Generator:

The following figure shows an example of the link training sequence for USB 3.0 on Analyzer:
Link Training USB 3.0 and USB 3.1 Parameters

The following table shows the parameters which can be configured for link training USB 3.0 and USB 3.1:

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Values</th>
<th>Default</th>
<th>Description</th>
<th>Applicable for USB LTSSM 3.0 / 3.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUT Type</td>
<td>Host, Device</td>
<td>Device</td>
<td>Specifies which role the BERT should play during link training. It can be either an downstream port (Host) or an upstream port (Device)</td>
<td>Both</td>
</tr>
<tr>
<td>Target State</td>
<td>LoopbackViaPolling, LoopbackViaPolling</td>
<td>LoopbackViaPolling</td>
<td>Determines the target state when bringing up the link</td>
<td>Both</td>
</tr>
</tbody>
</table>
### Trigger State

<table>
<thead>
<tr>
<th>Trigger State</th>
<th>XML: triggerState</th>
<th>RxDetectReset</th>
<th>RxDetectActive, PollingLFPS, PollingRxEq, PollingActive, PollingConfiguration, U0 RecoveryActive RecoveryConfiguration LoopbackActive PollingLFPSPlus PollingPortMatch PollingPortConfig, LoopbackActive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>This parameter determines when the trigger output signal of the LTSSM block should be asserted. Additionally this information can be translated into a trigger pulse on entering or leaving the specified state. This is done by the pulse shaper of the Ctrl Out A connector and no direct functionality of the LTSSM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Both</td>
</tr>
</tbody>
</table>

#### LFPS

<table>
<thead>
<tr>
<th>LFPS</th>
<th>tPeriod</th>
<th>XML: lfps_tPeriod</th>
<th>10 ns – 110 ns</th>
<th>50 ns</th>
<th>Period and Duty cycle of LFPS cycle</th>
<th>Both</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Duty Cycle</td>
<td>XML: lfps_dutyCycle</td>
<td>40 % - 60 %</td>
<td>50 %</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Polling.LFPS</td>
<td>tBurst</td>
<td>XML: pollingLFPS_tBurst</td>
<td>0.5 µs – 2 µs</td>
<td>1 µs</td>
<td>Link Training handshake before 5Gb/s</td>
<td>USB 3.0</td>
</tr>
<tr>
<td></td>
<td>tRepeat</td>
<td>XML: pollingLFPS_tRepeat</td>
<td>5 µs – 20 µs</td>
<td>10 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Warm Reset LFPS</td>
<td>tBurst</td>
<td>XML: warmResetLFPS_tBurst</td>
<td>80 ms – 120 ms</td>
<td>100 ms</td>
<td>LFPS trigger transition to Rx.Detect</td>
<td>Both</td>
</tr>
<tr>
<td>SCD1 and SCD2</td>
<td>tBurst</td>
<td>XML: scd1scd2_tBurst</td>
<td>0.5 µs – 1.5 µs</td>
<td>1 µs</td>
<td>SuperSpeedPlus Capability Declaration (SCD) is a step for a SuperSpeedPlus port, while in the Polling.LFPS substate, to identify itself as SuperSpeedPlus capable by transmitting Polling.LFPS signals with specific patterns unique to SuperSpeedPlus ports.</td>
<td>USB 3.1</td>
</tr>
<tr>
<td></td>
<td>tRepeat0</td>
<td>XML: scd1scd2_tRepeat-0</td>
<td>4 µs – 11 µs</td>
<td>7.5 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>tRepeat1</td>
<td>XML: scd1scd2_tRepeat-1</td>
<td>9 µs – 16 µs</td>
<td>12.5 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SuperSpeedPlus LFPS Based PWM Message (LBPM)</td>
<td>tPWM</td>
<td>XML: superSpeedPlus_tPWM</td>
<td>1.9 µs – 2.5 us</td>
<td>2.2 µs</td>
<td>LBPM is defined as a low power signaling mechanism for two SuperSpeedPlus ports to communicate with each other based on LFPS signals. The adoption of Pulse Width Modulation (PWM) is to embed the transmitting clock in data and to allow for easy data recovery at the receiver based on LFPS clock.</td>
<td>USB 3.1</td>
</tr>
<tr>
<td></td>
<td>tLFPS-0</td>
<td>XML: superSpeedPlus_tLFPS-0</td>
<td>0.4 µs – 0.9 us</td>
<td>0.750 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>tLFPS-1</td>
<td>XML: superSpeedPlus_tLFPS-1</td>
<td>1.23 µs – 1.9 us</td>
<td>1.450 µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Test Setup

Test Setup Requirements

The following are the test setup requirements to perform a USB link training:

- Keysight M8020A High Performance Serial BERT with a M8041A module
- One Keysight U7242A Fixture
- One 6 inch USB 3.0 cable
- Four SMA cables
- Four 11742A blocking capacitor

M8020A Setup

The following figure illustrates M8020A device setup to perform a USB link training:
The following figure illustrates M8020A host setup to perform a USB link training:

![USB Link Training Setup](image)

**Link Training Configuration**

You can configure the link training parameters to control LTSSM using the Sequence Settings window. For details on link training parameters, see Link Training Configuration on page 401.

USB 3.0 and 3.1 link training is possible with every channel of a M8041A and M8051A module.

**Test Procedure**

Follow the given steps to perform link training:

1. Load the instrument state in the M8070B software.
2. Power on the DUT.
3. Enable the Outputs of the M8041A.
4. Reset the DUT (disconnect/connect power at the fixture).
5. With this instrument setup everything is prepared for capturing the data. Hit the **Break** button in the Sequence Editor to start the link training. If link training is successful, the **Status Indicator** should show that the sequencer of the generator is executing the last block and that there are no bit errors.

6. For shutting down the link hit the **Break** button again. The sequencer of the generator should return to block 2.

7. Press **Break** button again for starting the link training again.
Link Training Log

The Link Training Log window displays the log generated while initiating the link training test for USB 3.0 and USB 3.1. All information regarding the executed tests and their status are displayed with the date and time stamp. This helps to identify the root cause of a problem. For instance, the Link Training Log shows test failure due to an unexpected LTSSM state change.

The following figure shows the log generated while initiating the link training test for USB 3.0:

The following figure shows the log generated while initiating the link training test for USB 3.1:
You can open/close the **Link Training Log** window by clicking on the **Show/Hide Link Training Log** icon present in the status bar. The **Show/Hide Link Training Log** icon with orange background indicates an update or new entry in the link training log.

**M8070B Support for PCIe3.0/4.0/5.0 Link Training using M8040A**

The M8040A supports interactive link training for PCIe3.0, PCIe4.0, and PCIe5.0. This section describes the M8070B support to conduct PCIe3.0/4.0/5.0 link training by M8040A (M8145A & M8046A) modules.

**Hardware Setup**

Using the interactive link training on M8040A requires a M8045A Pattern Generator module equipped with at least one Data Out and a M8046A Error Detector module.

Both Pattern Generator and Error Detector modules need to be equipped with a (Sequence) Link Connector on their front panels.

For Error Detector module, it is a requirement to be equipped with a built-in CDR, these modules also support the Sequence Link connector.

For Pattern Generator modules, every Data Out has its own Link port. Which PG Data Out Link connector is connected to which Error Detector Data In Link connect is queried automatically by the instrument and cannot be specified manually. It is also automatically detected, if a link cable is removed and the link is re-established before another link training run is performed.

The cable part number M8041-61601 is required to connect two link connectors.

Interactive link training is used on each of the two Data Outs of a M8040A Pattern Generator module, therefore two DUTs can be trained in parallel when additionally using two M8040A Error Detector modules.

As there is only one differential Trig Out connector on a M8040A Pattern Generator module, though using two DUTs in parallel requires splitting the signal by some means to be able to supply two compliance boards with a reference clock.
Licensing

Required Options

<table>
<thead>
<tr>
<th>License</th>
<th>Instrument Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8045A-G32</td>
<td>G32</td>
<td>32Gbaud PG</td>
</tr>
<tr>
<td>M8045A-0G4</td>
<td>0G4</td>
<td>De-emphasis</td>
</tr>
</tbody>
</table>

The minimum M8040A configuration requires options G32 and 0G4 for the PG. De-emphasis optimization is an essential part of PCIe link training.

<table>
<thead>
<tr>
<th>License</th>
<th>Instrument Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8046A-A32</td>
<td>A32</td>
<td>32Gbaud ED</td>
</tr>
<tr>
<td>M8046A-0A3</td>
<td>0A3</td>
<td>Equalizer</td>
</tr>
<tr>
<td>M8046A-0A4</td>
<td>0A4</td>
<td>Clock Recovery for 32 Gbaud</td>
</tr>
<tr>
<td>M8046A-0S1</td>
<td>0S1</td>
<td>Interactive Link Training for PCIe 8/16/32 GT/s</td>
</tr>
<tr>
<td>M8046A-0S2</td>
<td>0S2</td>
<td>SKP OS Filtering for PCIe 8/16/32 GT/s and CCIX 20/25 Gb/s</td>
</tr>
</tbody>
</table>

The minimum M8040A ED configuration requires options A32 and 0A4 for being able to capture data using the CDR at up to 32 Gb/s.

Additionally, options 0A4 for clock recovery, 0S1 for PCIe link training, and option 0S2 for SKP OS filtering are required.

Recommended Options

These options are not absolutely required for LTSSM usage, but are needed for performing full verification of PCIe functionality of a DUT.

<table>
<thead>
<tr>
<th>License</th>
<th>Instrument Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8045A-0G3</td>
<td>0G3</td>
<td>Jitter</td>
</tr>
<tr>
<td>M8045A-0G6</td>
<td>0G6</td>
<td>Reference Clock Input with Multiplying PLL</td>
</tr>
</tbody>
</table>
Recommended Packages

To be able to perform a jitter tolerance, bathtub, etc. measurement for DUT debugging/characterization, it is advantageous to have the Advanced Measurement Package for M8000 Series BERT Test Solutions (M8070ADVB).

Sequence Editor

Using PCIe LTSSM functionality

The interactive link training functionality is specified differently by selecting a PHY Protocol from the Sequence Configuration block.

Doing this will show or hide various other sequence specific properties which are only valid for a specific PHY Protocol.

M8040A PG

The following additional features will appear in the Sequence Editor, only when selecting one of the PCIe PHY Protocol options inside of sequences which are bound to M8040A PG Data Out locations.

PCIe3.0/4.0/5.0

Link Training PCIe – Allows to modify properties of the link training procedure.

Link Training Sequence Block Type – Perform Link Up/Down

Link Training Trigger – Enable trigger signal asserted on a specific LTSSM state

Link Training Block Branch Events – Perform sequence branching on specific LTSSM events
These features are described in further detail below.

**M8040A ED**

On the error detector the functionality, supporting interactive link training is different compared to the pattern generator.

**PCle3.0/4.0/5.0 and CCIX**

For these PHY Protocol selections SKP OS filtering is automatically enabled. It removes SKP OS symbols contained in the data stream before measuring BER. Doing this is required as the BER is measured against a static memory pattern, but the number of SKP OS symbols contained in the received data stream (sent by a DUT) is variable.

**PCle3.0/4.0/5.0**

Link Training Block Branch Events – Perform sequence branching on certain LTSSM events

**XML Sequence Description**

The PHY Protocol for PCIe5 mode is specified the following way.

```
<linkTrainingConfigurations>
  <pcie3 capability="PCle5"/>
</linkTrainingConfigurations>
```

Specifying any of the other PHY protocol modes (e.g. PCIe3 or PCIe4) works accordingly.

The way of specifying the used LTSSM type inside the sequence XML description is backwards compatible to M8020A. Therefore, an already existing M8020A sequence can be reused on a M8040A module without any changes when programmed via SCPI.

For the `<pcie3/>` node attributes other than “capability” are ignored by M8040A ED modules as these attributes control the LTSSM which driven by the M8040A PG.

**Link Training sequence block type**

A special “Link Training” sequence block type is selectable for sequences bound to M8040A PG locations.

These blocks are used to either start link training up (Link Training block with direction “Up”) to the selected target speed or disable the link (Link Training block with direction “Down”).
Selection of Link Training block type and settings

Representation of Link Training block in graphical sequence view

XML Sequence Description

In the sequence XML a LinkTraining Block is defined by using the <linkTraining/> node.

```xml
<sequence>
  <loop>
    <block length="1024" name="LinkTrainingDown">
      <linkTraining direction="down"/>
    </block>
  </loop>
</sequence>
```
7 Setting up Patterns

**Link Training Sequence Controls**

Link Training Trigger

![Link Training Trigger](image)

**Link Training Events**

Detect State – Link Training

Target State – Link Training

Error State – Link Training

![Link Training Events](image)
Scrambler and EI EOS

There is currently no scrambler implemented in M8040A. The EI EOS symbols are derived automatically from the selected PCIe generation.

Link Training PCIe

**Generation**

In contrast to M8020A, this parameter cannot be defined separately and is always derived off the PHY protocol selection. Possible values are either PCIe3/4 or 5.

**User Calibrated Presets**

This legacy M8020A parameter is not available for M8040A, presets are user defined at the respective Data Out and therefore always custom/calibrated.

In case a Data Out is part of a sequence with the PHY Protocol selected as PCIe, the Deemphasis functional block of the channel changes into the PCIe LTSSM preset mode.

With these outputs-specific parameters, it is possible to define the used full swing value and use potentially calibrated deemphasis cursor settings.

**PCIe3 and PCIe4**

When using PCIe3 or PCIe4, the parameters are generally the same as with M8020A modules.

**Lane**

The only allowed value for this field is still 0.

**Select Start Preset Gen 4**

In contrast to M8020A, it is now possible to specify the additional parameter value LTSSM Defined.

- **User Defined**
  Same as M8020A
7 Setting up Patterns

- **LTSSM Defined**
  This new parameter value uses the setting determined by the LTSSM during Gen 3 training.

**PCIe5**
Starting with M8040A, it is possible for the first time to do link training for PCI Express up to generation 5.

Most of the parameters are the same than with PCIe3 and 4 but some new parameters were introduced and changed.

**Lane**
When doing PCIe5 is now possible to use the values 0 to 31 for specifying a lane.

**Select Start Preset Gen 5**
- **User Defined**
  Uses preset value selected in ‘Start Preset Gen 4’ parameter
- **LTSSM Defined**
  Use the value determined by the LTSSM during Gen4 training
**PCle LTSSM Parameters**

The parameters used to control the PCle LTSSM are shown in the following figure:
## General Parameters

These parameters are required for general setting up the LTSSM operation.

<table>
<thead>
<tr>
<th>Name</th>
<th>Possible Values</th>
<th>Description</th>
<th>Used for DUT type</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUT Type</td>
<td>Add-in card</td>
<td>Specifies which role the BERT should play during link training. It can</td>
<td>Both</td>
</tr>
<tr>
<td></td>
<td>System Board</td>
<td>either be an upstream device for testing a downstream port or vice versa.</td>
<td></td>
</tr>
<tr>
<td>Target Speed</td>
<td>32.0 GT/s</td>
<td>Determines the target speed when doping the speed change.</td>
<td>Both</td>
</tr>
<tr>
<td></td>
<td>16.0 GT/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8.0 GT/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Target State</td>
<td>Loopback via</td>
<td>Determines the target state when bringing up the link.</td>
<td>Both</td>
</tr>
<tr>
<td></td>
<td>Recovery</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Loopback via</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trigger State</td>
<td>Trigger States</td>
<td>This parameter determines when the trigger output signal of the LTSSM</td>
<td>Both</td>
</tr>
<tr>
<td></td>
<td></td>
<td>block should be asserted. Additionally, this information can be</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>translated into a trigger pulse on entering or leaving the specified state.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This is done by the pulse shaper of the TCRL OUT connector and no direct</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>functionality of the LTSSM.</td>
<td></td>
</tr>
<tr>
<td>Compliance</td>
<td>Deasserted</td>
<td>Specifies whether the compliance received bit is asserted or</td>
<td>Both</td>
</tr>
<tr>
<td>Receive Bit</td>
<td>Asserted</td>
<td>de-asserted in TS1.</td>
<td></td>
</tr>
<tr>
<td>Ref Clock Architecture</td>
<td>Common,</td>
<td>Defines the PCIe Reference Clock Architecture - common reference</td>
<td>Both</td>
</tr>
<tr>
<td></td>
<td>Separate</td>
<td>clock / separate reference clock.</td>
<td></td>
</tr>
<tr>
<td>Link EQ states</td>
<td>Bypass</td>
<td>Determines whether link equalization should be performed. It can either</td>
<td>Both</td>
</tr>
<tr>
<td></td>
<td>Presets only</td>
<td>either be aborted after phase 1 (Bypass) or fully executed. In the second</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>case it can be determined whether only preset or all (i.e. individual cursor)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>requests should be accepted.</td>
<td></td>
</tr>
<tr>
<td>Lane Number</td>
<td>0-31</td>
<td>The lane number being used.</td>
<td>Both</td>
</tr>
<tr>
<td>Link Number</td>
<td>0-255</td>
<td>The link number being used.</td>
<td>Add-in Card†</td>
</tr>
<tr>
<td>BERT Start Preset Gen3</td>
<td>P0-P9</td>
<td>This is the preset used by the BERTs TX port after switching to Gen 3</td>
<td>Add-in Card</td>
</tr>
<tr>
<td></td>
<td></td>
<td>operation and when operating as an upstream device.†</td>
<td></td>
</tr>
<tr>
<td>RX Preset Hint</td>
<td>0 (-6 dB)</td>
<td>This is the preset hint being sent by the BERT to the DUT during phase 0</td>
<td>Add-in Card</td>
</tr>
<tr>
<td></td>
<td>1 (-7 dB)</td>
<td>of the link equalization procedure. It's only used when the BERT operates</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 (-8 dB)</td>
<td>as upstream device.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 (-9 dB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4 (-10 dB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5 (-11 dB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>6 (-12 dB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7 (reserved)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Name</td>
<td>Possible Values</td>
<td>Description</td>
<td>Used for DUT type</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>-----------------</td>
<td>------------------------------------------------------------------------------</td>
<td>-------------------</td>
</tr>
<tr>
<td>DUT Start Preset Gen3</td>
<td>P0-P9</td>
<td>This is the preset the BERT transfers to the DUT in phase 0 of the link equalization procedure. It's only used when the BERT operates as an upstream device (2.5G to 8G)</td>
<td>Add-in Card</td>
</tr>
<tr>
<td>DUT Target Preset Gen3</td>
<td>P0-P9, Cursor</td>
<td>This is the preset the BERT requests the DUT to switch to during link equalization. Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training (8G)</td>
<td>Both</td>
</tr>
<tr>
<td>Select BERT Start Preset Gen4</td>
<td>User Defined</td>
<td>Use BERT start preset specified by user or use resulting preset of phase 2 of 8GT/s TXEQ as start preset.</td>
<td>Add-in Card</td>
</tr>
<tr>
<td>BERT Start Preset Gen4</td>
<td>P0-P9</td>
<td>This is the preset used by the BERTs TX port after switching to Gen4 operation and when operating as an upstream device.</td>
<td>Add-in Card</td>
</tr>
<tr>
<td>DUT Start Preset Gen4</td>
<td>P0-P9</td>
<td>This is the preset the BERT transfers to the DUT in phase 0 (Gen4) of the link equalization procedure. It's only used when the BERT operates as an upstream device.</td>
<td>Add-in Card</td>
</tr>
<tr>
<td>DUT Target Preset Gen4</td>
<td>P0-P9, Cursor</td>
<td>This is the preset the BERT requests the DUT to switch to during link equalization (Gen4). Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training.</td>
<td>Both</td>
</tr>
<tr>
<td>Select BERT Start Preset Gen5</td>
<td>User Defined</td>
<td>Use BERT start preset specified by user or use resulting preset of phase 2 of 16GT/s TXEQ as start preset.</td>
<td>Add-in Card</td>
</tr>
<tr>
<td>BERT Start Preset Gen5</td>
<td>P0-P9</td>
<td>This is the preset used by the BERTs TX port after switching to Gen5 operation and when operating as an upstream device.</td>
<td>Add-in Card</td>
</tr>
<tr>
<td>DUT Start Preset Gen5</td>
<td>P0-P9</td>
<td>This is the preset the BERT transfers to the DUT in phase 0 (Gen5) of the link equalization procedure. It's only used when the BERT operates as an upstream device.</td>
<td>Add-in Card</td>
</tr>
<tr>
<td>DUT Target Preset Gen5</td>
<td>P0-P9, Cursor</td>
<td>This is the preset the BERT requests the DUT to switch to during link equalization (Gen5). Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training.</td>
<td>Both</td>
</tr>
<tr>
<td>DUT Target Pre-Cursor @ Target Speed</td>
<td>0-63</td>
<td>This is the pre-cursor value that the BERT requests the DUT to use during link equalization in cursor mode at Target Speed. Depends on the role the BERT is playing this is done in either phase 2 or 3 of the link equalization training. If not specified 0 is used.</td>
<td>Both</td>
</tr>
<tr>
<td>DUT Target Main-Cursor @ Target Speed</td>
<td>0-63</td>
<td>This is the main cursor value that the BERT requests the DUT to use during link equalization in cursor mode at Target Speed. Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training. If not specified 63 is used.</td>
<td>Both</td>
</tr>
</tbody>
</table>
### Static Parameters

**The Low Frequency Parameter**

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LF</td>
<td>8</td>
<td>The value which corresponds to the minimum differential value that can be generated by the transmitter.</td>
</tr>
</tbody>
</table>

### Parameters being controlled by the Sequencer

These parameters are required for testing, but are controlled by the Sequencer. So they are not direct input parameters of the LTSSM.

<table>
<thead>
<tr>
<th>Name</th>
<th>Possible Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUT Test Pattern</td>
<td>Compliance Test Pattern, Modified Compliance Pattern</td>
<td>Specified the test pattern being sent out by the Sequencer when the link is up (i.e. LTSSM is in loopback state).</td>
</tr>
</tbody>
</table>
LTSSM States

LTSSM transits through various states and substates during link initialization, training, and management. The entry and exit of each of these states and the exchange of packets (Ordered sets) between the two devices during each state are as per the PCIe specifications. Following is a list of these states as per the PCIe specifications.

<table>
<thead>
<tr>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detect.Active</td>
</tr>
<tr>
<td>Polling.Active</td>
</tr>
<tr>
<td>Polling.Configuration</td>
</tr>
<tr>
<td>Configuration.Linkwidth.Start</td>
</tr>
<tr>
<td>Configuration.Linkwidth.Accept</td>
</tr>
<tr>
<td>Configuration.Lanenum.Wait</td>
</tr>
<tr>
<td>Configuration.Lanenum.Accept</td>
</tr>
<tr>
<td>Configuration.Complete</td>
</tr>
<tr>
<td>Configuration.Idle</td>
</tr>
<tr>
<td>L0</td>
</tr>
<tr>
<td>Loopback.Active</td>
</tr>
<tr>
<td>Recovery.Equalization.Phase0</td>
</tr>
<tr>
<td>Recovery.Equalization.Phase1</td>
</tr>
<tr>
<td>Recovery.Equalization.Phase2</td>
</tr>
<tr>
<td>Recovery.Equalization.Phase3</td>
</tr>
<tr>
<td>Recovery.Speed</td>
</tr>
</tbody>
</table>

For details on LTSSM states, see LTSSM States on page 466.
Using M8062A Data Out Squelch Feature

This M8062A Data Out squelch feature is used to squelch the M8062A’s Data Out signals as specified in the selected pattern file.

Limitations

Following are the limitations of this feature:

- Minimum duration of signal squelch is 40 ns
- The squelch effects turn on/off only occurs on a raster of 10 ns.
- The squelch duration can only be modified in the granularity of a Symbol Width dependent bit raster
- Squelch/Data accuracy is ± 2 hardware word widths as defined in Table 63 on page -501.
- Inversion switch of Ctrl Out A signal is not supported when using squelch

Hardware Requirements

To use this feature, the M8041A module must be coupled with a M8062A module.

Hardware Setup

To use this feature it is required to connect the predefined cable (M8046A-801) from Ctrl Out A of the M8040A module to the Electrical Idle In of the M8062A module.

Software Usage

Following the given steps to use the M8062A Data Out squelch feature though M8070B software:

1. From the Modules View, activate the Ctrl Out A output of the M8041A module (M1).
2 Change the electrical idle input (squelch input) setting of the M8062A module (M2) to External. This is for external signal to have any effect on the M8062A's Data Out.

3 More settings for the **Electrical Idle In** can be changed by selecting the respective module location configured with Elect Idle In.

4 Open the **Sequence Editor**. The squelch can be activated by adding a **Sequence Control** to the M8062A Data Out sequence. Select the **Target** as **Ctrl Out A**, the **Module** as **M2** (the only valid selection with M8062A usage) and the **Source** as **Squelch**.

5 Alternatively for activating this feature in the GUI it is also possible to specify this setting directly in the XML definition of the sequence. With this it also is possible to activate this feature via SCPI:
6 Open the **Pattern Editor** window. When creating a new pattern it is necessary to activate squelch information bits in the pattern. This allows definition of squelched bits by pressing the **S** key or using the respective GUI button. The squelched bits are then underlined by a yellow line.
When defining a pattern containing signal squelching for usage with M8062A it is required to always squelch two bits in a row. This is necessary because the pattern will be downloaded independently into Channel 1 and Channel 2 of the M8041A module driving the M8062A. By squelching a single bit the whole word will be squelched. Effective word widths used by the hardware depend on the Symbol Width setting in the Sequence Editor.

![Sequence Editor with Symbol Width set to 130](image)

The selection thereby results in the following hardware word width for M8041A/M8062A.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>64</td>
<td>128</td>
</tr>
<tr>
<td>10</td>
<td>80</td>
<td>160</td>
</tr>
<tr>
<td>130</td>
<td>130</td>
<td>260</td>
</tr>
<tr>
<td>132</td>
<td>132</td>
<td>264</td>
</tr>
</tbody>
</table>

For signal squelching to work reliably, it is required that the resulting duration of the squelched blocks is at least 20 ns in length. Otherwise, the Electrical Idle In of the M8062A might miss a signal from the M8041A’s Ctrl Out A port.

The minimum granularity of a squelch signal is limited by the currently used word width of the M8041A/M8062A combination.
M8046A PHY Protocol Selection (SKP OS Filtering)

PHY Protocol

The M8046A modules allows to specify a PHY protocol which can be supported by a specific sequence. This selection is done in the Sequence Editor when selecting a sequence which is bound to a module supporting this feature.

From the Sequence Editor, go to the Sequence Configuration block in the Sequence Properties side pane and select a PHY Protocol.
The available choices depend on the channels using the sequence.

For M8046A, following are the possible options:

- **M8046A-0S2 (US2, TS2)**: SKP OS Filtering for PCIe. This includes 8b10b and 128b130b coding.
  
  The available PHY protocol selections for this license are as follows:
  
  - None - No specific sequence capability
  - CCIX - Dedicated sequence setting for CCIX
  - PCIe2 - Dedicated sequence setting for PCIe2
  - PCIe3 - Dedicated sequence setting for PCIe3
  - PCIe4 - Dedicated sequence setting for PCIe4
  - PCIe5 - Dedicated sequence setting for PCIe5

- **M8046A-0S4 (US4, TS4)**: SKP OS Filtering for USB. This includes 8b10b and 128b132b coding.
  
  The available PHY protocol selections for this license are as follows:
  
  - USB 3.0 - Dedicated sequence setting for USB 3.0
  - USB 3.1 - Dedicated sequence setting for USB3 3.1

- **M8046A-0S6 (US6, TS6)**: SKP OS Filtering for PCIe. This includes 8b10b and 128b150b coding.
  
  The available PHY protocol selections for this license are as follows:
  
  - SATA3 - Dedicated sequence setting for SATA3
  - SAS2 - Dedicated sequence setting for SAS2
  - SAS3 - Dedicated sequence setting for SAS3

The PHY Protocol selection automatically defines the alignment, filler symbol sequences for the selected standard.

There is no option to manually enter these symbols on a sequence for a M8046A.

All of the above selected protocols have the single additional feature that SKP OS filtering is active as soon as the sequence is downloaded.

All of the modules bound to this sequence need to be capable of supporting this feature.

**NOTE**

When selecting a specific PHY protocol on M8046A the maximum allowed data rate is 32.4 Gb/s.
SKP Ordered Set filtering/removal

The M8046A module supports SKP OS filtering for the PCIe3, PCIe4, PCIe5 and CCIX standards as defined in the respective specification.

**NOTE**
Scrambler will not be available for M8040A.

**NOTE**
Selection of PCIe 5 is supporting SKP OS symbol filtering as defined in version 0.7.

**NOTE**
SKP OS filtering is available as per installed licenses (OS2, OS4, OS6 and the corresponding upgrade, or trial licenses).

For the new module specific options, please refer to M8040A Licenses on page 557.

This functionality removes all SKP ordered sets from the received data stream. When setting up a sequence for a BER measurement which is bound to the Error Detectors Data In it is required for the pattern to not contain any SKP OS symbols. As these symbols are removed before comparing the received and expected data.

The SKP OS filtering functionality does not discriminate between the different standards but removes all possible SKP OS symbol types in the above mentioned standards.
In case SKP OS filtering is active the expected pattern must not contain any SKP OS symbols as these will get removed before the received data stream is compared to the expected pattern.

Whenever a SKP OS symbol is removed from the received data stream the expected pattern compare position is pinned down until past the SKP OS symbols duration to be able to compare the data. The necessity for modifying the compare position leads to the need to do a (manual or automatic) pattern re-sync whenever a SKP OS symbol is not recognized by the analyzer. For example because of a bit error or a wrong threshold setting.

Setting up SKP OS filtering

The following picture shows how to setup SKP OS filtering for the CCIX standard when using M8045A and M8046A.

On the Generator pattern, open Factory Patterns dialog and then navigate to e.g. CCIX/Test and select either:

- CCIX_modified_compliance_lane_0_CC_BIT_20G_25G
- CCIX_modified_compliance_lane_0_IR_BIT_20G_25G
The pattern selection depends on whether the DUT uses a common clock (CC) or derives its own independent reference (IR) clock.

On the Analyzer pattern, open Factory Patterns dialog and then navigate to e.g. CCIX/Test. For the Analyzer pattern there is just a single pattern:

- CCIX_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_20G_25G

It is required as the difference between the CC and IR generator pattern files lies in the SKP OS symbol count which are getting removed before measuring the BER.

The above pattern is made specifically to fit to the M8046A modules memory granularity.
8 Working with Measurements

Overview / 508
Exploring Measurement User Interface / 509
Error Ratio Measurement / 515
Overview

The M8070B system software provides the following types of measurements:

- Error Ratio
- Parameter Sweep

In addition, the M8070B system software also provides the following measurements will be only available on installing the following plugins:

- **Advanced Measurement Package**
  The **Advanced Measurement Package** provides the following measurements:
  - Output Timing
  - Output Level
  - Jitter Tolerance
  - Eye Diagram

  For details on the measurements provided by **Advanced Measurement Package**, please refer to **M8000 Series Advanced Measurement Package User Guide**.

- **Error Distribution Analysis Package**
  The **Error Distribution Analysis Package** provides the following measurement:
  - Error Distribution Analysis

  For details on the measurement provided by **Error Distribution Analysis Package**, please refer to **M8000 Series Error Distribution Analysis Package User Guide**.

**NOTE**

Please note that the M8046A module only supports the following measurements:

- Error Ratio
- Output Timing
- Jitter Tolerance
Exploring Measurement User Interface

This section describes the functionality provided by the measurement user interface.

Launching the Measurement User Interface

To launch the measurement user interface:

- Go to the **Menu Bar > Measurements** and then select the respective measurements (**Error Ratio**, **Output Timing**, **Output Level** or **Jitter Tolerance**) to launch the measurement user interface.

The following figure shows the measurement user interface:

![Measurement User Interface Diagram]

The measurement user interface has the following GUI elements which are common to all measurements:

- Toolbar
- Status Indicator
- Measurement History Pane
- Measurement Graph
- Parameter Window
- Calculated Results Pane
Let's discuss these GUI elements in the following sections.

### Toolbar

The toolbar contains the following icons:

<table>
<thead>
<tr>
<th>Elements</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Start /Continue Measurement</td>
<td>Starts a measurement.</td>
</tr>
<tr>
<td></td>
<td>Break Measurement</td>
<td>Halts the measurement at that point. Once paused, you can continue the measurement again by pressing Continue Measurement icon. Note: This option is not available in Error Ratio Measurement.</td>
</tr>
<tr>
<td></td>
<td>Stop Measurement</td>
<td>Stops the measurement.</td>
</tr>
<tr>
<td></td>
<td>Step Into Measurement</td>
<td>Steps further into the measurement. Note: This option is not available in Error Ratio Measurement.</td>
</tr>
<tr>
<td></td>
<td>Enable/Disable Measurement Run History</td>
<td>Enables or disables the measurement run history. For details, refer to Measurement History Window on page 511.</td>
</tr>
<tr>
<td></td>
<td>Clear Measurement History</td>
<td>Clears the measurement run history.</td>
</tr>
<tr>
<td></td>
<td>Copy Measurement History Properties</td>
<td>Copies the measurement history properties to the currently running measurement.</td>
</tr>
<tr>
<td></td>
<td>Reset Measurement</td>
<td>Resets the measurement to its default values.</td>
</tr>
</tbody>
</table>
Status Indicator

The status indicator shows the current state of a measurement. There can be various states of a measurement, depending on the type of measurement. These may be as follows:

- **Not Started**: Indicates that the measurement has not yet started.
- **Running**: Indicates that the measurement is currently running.
- **Stop**: Indicates that the measurement is stopped.
- **Error**: Indicates an error while executing the measurement which is caused due to invalid parameter settings.
- **Suspended**: Indicates that the measurement is suspended.
- **Finished**: Indicates that the measurement is completed.

The following figure shows the status indicator while the measurement is running:

![Running Status Indicator](image)

Measurement History Window

The **Measurement History** window maintains the history of executed measurement along with their time stamp. This allows you to refer to the previously run measurements and compare their results.

The **Measurement History** window is shown in the figure below:

![Measurement History Window](image)

Click the icon to toggle between the enable/disable measurement run history in the Measurement History window.
Copy Measurement History Properties

This feature allows you to copy the properties of run measurement to currently running measurement.

To do so,

• Select a measurement history from the list shown in the Measurement History window.

• Click the Copy Measurement History Properties icon. The properties of the selected measurement will be copied to the current measurement.

Measurement Graph

The Measurement Graph displays the calculated graph and results. The following figure displays the Measurement Graph of the Output Timing Measurement.
The **Measurement Graph** contains the following tabs:

- **Graph**: Displays the graphical representation of the measurement. The graph varies from measurement to measurement. The details of each measurement graph are further described in their respective sections.

- **Location**: Displays the raw measurement data for that location. However, if you are running measurement for a group, multiple tabs will appear that display the raw measurement for each location.

When you right-click on the **Measurement Graph**, a context menu appears which provides the following options:

- **Turn ON/OFF Fit to view (Ctrl+Home)** - Turns ON/OFF Fit to view option.

- **Fit to view (Home)** - Makes the visible area fit to display entire contents.

- **Copy screenshot (F11)** - Copies the screenshot of charts to clipboard.

- **Save screenshot (Ctrl+S)** - Saves the screenshot as an image (PNG) under a name.

Clicking this option displays the **Save Screenshot As** dialog box.

![Save Screenshot As](image)

- On the **Save Screenshot As** dialog box, select one of the following:
  - **Displayed**: Saves the screenshot with default properties.
  - **Custom**: Enables you to set the custom properties of the image. The following properties are available:
    - **Width**: Sets the width value of the image.
    - **Height**: Sets the height value of the image.
    - **Color Scheme**: Enables you to select a color scheme for the image. Two options; Dark and Light are available.
• **Show Legends**: Allows you to save the legends in the screenshot.
  
  b. Click **OK** to save the screenshot.

• **Quick Help (Alt+F1)** - Opens a window that provides brief information about the dynamic display.

### Parameters Window

The **Parameter** window allows you to set the parameters for a location or a group. For each measurement, it contains two types of parameters:

- **Acquisition Parameters** - Pre-Parameters influence how the data for a measurement is collected; changes require a re-run in order to be effective. It also allows you to select a location or location group against which the data acquisition is performed.

- **Evaluation Parameters** - Post-Parameters influence how the collected measurement data is evaluated. Changes do not require a re-run in order to be effective.

The acquisition and evaluation parameters differ from measurement to measurement. The detailed description of these parameters are explained in the sections that follow.

### Calculated Results Pane

The **Calculated Results** pane displays the calculated results in the form of measurement parameters for each location. The calculated measurement parameters varies from measurement to measurement.

The **Calculated Results** pane is shown in the following figure:

For each location, you can click on the slide button to show/hide the measurement graph.
Error Ratio Measurement

Overview

The Error Ratio Measurement allows you to collect measurement data over a specific period. This can be used to create test scenarios that are reproducible and comparable. Also, you can let tests run over long times and then evaluate the results afterwards.

NOTE
While the error ratio measurement is running, you should not modify the measurement setup, as the measured bit errors do not represent the performance of your DUT under real circumstances.

The period of time can be set through the Parameters window, an absolute time setting, or the time it takes to measure a specified number of bits or bit errors. The accumulation period should be long enough to make a statistically valid BER measurement.

Launching Error Ratio Measurement

To launch the Error Ratio Measurement:

- Go to the Menu Bar &gt; Measurements and then select Error Ratio.

The user interface of Error Ratio Measurement will appear as shown in the following figure:
The **Error Ratio** user interface includes the following elements:

- **Toolbar**: For details, refer to [Toolbar](#) on page 510.
- **History Pane**: For details, refer to [Measurement History Window](#) on page 511.
- **Measurement Graph**: For details, refer to [Measurement Graph](#) on page 520.
- **Parameter Pane**: For details, refer to [Acquisition and Evaluation Parameters for Error Ratio](#) on page 517.
- **Calculated Results**: For details, refer to [Calculated Results](#) on page 522.
Acquisition and Evaluation Parameters for Error Ratio

The **Parameters** window allows you to set the acquisition and evaluation parameters for **Error Ratio** measurement:

**Table 65**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Acquisition Parameters</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analyzer Location</td>
<td>Location or location group against which the data acquisition is performed.</td>
<td>Use the drop-down list to specify the location or location group.</td>
</tr>
<tr>
<td>Accumulation End</td>
<td>Specify the criteria to end accumulation.</td>
<td>Pass/Fail</td>
</tr>
<tr>
<td>Accumulation Duration</td>
<td>Specify the acquisition duration.</td>
<td>Fixed Time</td>
</tr>
<tr>
<td>Accumulation Fix Time</td>
<td>Specifies the duration of the accumulation.</td>
<td>Min - 1 s Max - 31.5 Ms</td>
</tr>
<tr>
<td>Accumulation Interval</td>
<td>Specify the accumulation interval on which the error ratio sample is taken.</td>
<td>Min - 100 ms Max - 2 Ms</td>
</tr>
<tr>
<td>Accumulation Stop Criteria</td>
<td>Specify the accumulation end criteria when measurement is run on a group of analyzers.</td>
<td>Per Analyzer</td>
</tr>
<tr>
<td>Number of Compared Bits</td>
<td>Specify the number of compared bits for which the error ratio sample is taken.</td>
<td>Min - 1E-6 Max - 1E+18</td>
</tr>
<tr>
<td>Target Error Ratio</td>
<td>Specifies the target error ratio of the accumulation results.</td>
<td>Min - 1E-18 Max - 1E-3</td>
</tr>
<tr>
<td>Target Confidence Level</td>
<td>Specifies the target confidence level of the accumulation results.</td>
<td>Min - 0.1 % Max - 99.9 %</td>
</tr>
</tbody>
</table>
How to Run a Measurement

The Error Ratio measurement immediately starts calculating the error ratio as soon as it receives a valid signal and the respective error ratio settings are done.

To run an Error Ratio measurement, perform the following steps:

- Use the Parameters window to select the location or location group for which the data acquisition has to be performed.
- Set the acquisition parameters in the Parameters window. For details, refer to Acquisition and Evaluation Parameters for Error Ratio on page 517.
- Click the Start Measurement icon to run the measurement. The measurement status indicator will indicate Running.

Please note that once you run the measurement you cannot modify the acquisition parameters. However, if you try to modify acquisition parameters by stopping the measurement and then run the measurement, a new instance of measurement will be executed.
Error Ratio Measurement with PAM4 Symbols

The M8040A modular system allows you to run the Error Ratio measurement using the PAM4 symbols. To do so,

- Switch to the Module View.
- From the Generator (M8145A), select Data Out location. Choose the Line Coding as PAM4 in the Parameter window.
- From the Analyzer (M8146A), select Data In location. Choose the Line Coding as PAM4 in the Parameter window.
- Once done, switch to Error Ratio measurement.
- Set the acquisition parameters in the Parameters window. For details, refer to Acquisition and Evaluation Parameters for Error Ratio on page 517.

- Click the Start Measurement icon to run the measurement. The measurement status indicator will indicate Running.
- The Display Error Ratio in the Parameter window will now show the error ratio for various symbol levels (0-3) as shown in the following figure:

![Display Error Ratio Figure]

- See Calculated Results on page 522 for the results which are displayed when an Error Ratio measurement is performed with PAM4 line coding.
How to Stop a Measurement

To stop an Error Ratio measurement:

- Click the Stop Measurement icon to stop the measurement.

Measurement Graph

Once you run an Error Ratio measurement for a specified duration, the calculated graph and the raw data is shown on the measurement graph as follows:

This graph displays the delta errored 1’s ratio, delta errored 0’s ratio, and total delta error ratio at data points over the entire accumulation period. The error ratios on the y-axis are set to a range of 1E+0 (100% errors) to 1E-12. The accumulation period is on the x-axis.
Display Change

During accumulation, data will appear to move from left to right on the ratios graph. When the graph is completely filling the display, the x-axis time scale will double. The data graph is then occupying only half of the display and will continue to move to the right again. This will repeat until the accumulation period has ended.

Measurement Data

The following figure shows the raw measurement data for the selected location.

<table>
<thead>
<tr>
<th>TimeStamp</th>
<th>Error Ratio</th>
<th>Compared Bits</th>
<th>Errored Bits</th>
<th>Error Zero Ratio</th>
<th>Compared Zeros</th>
<th>Errored Zeros</th>
<th>Error One Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>00:00:00:211</td>
<td>1.33e-08</td>
<td>1.00e+09</td>
<td>1.40e+00</td>
<td>7.64e-09</td>
<td>5.24e+08</td>
<td>4.00e+00</td>
<td>1.88e-08</td>
</tr>
<tr>
<td>00:00:00:415</td>
<td>5.89e-09</td>
<td>1.02e+09</td>
<td>6.00e+00</td>
<td>9.89e-09</td>
<td>5.06e+08</td>
<td>5.00e+00</td>
<td>1.95e-09</td>
</tr>
<tr>
<td>00:00:00:627</td>
<td>9.01e-09</td>
<td>1.11e+09</td>
<td>1.00e+01</td>
<td>1.27e-08</td>
<td>5.51e+08</td>
<td>7.00e+00</td>
<td>5.36e-09</td>
</tr>
<tr>
<td>00:00:00:845</td>
<td>9.61e-09</td>
<td>1.04e+09</td>
<td>1.00e+01</td>
<td>7.75e-09</td>
<td>5.16e+08</td>
<td>4.00e+00</td>
<td>1.14e-08</td>
</tr>
<tr>
<td>00:00:01:075</td>
<td>1.31e-08</td>
<td>1.15e+09</td>
<td>1.50e+01</td>
<td>8.78e-09</td>
<td>5.70e+08</td>
<td>5.00e+00</td>
<td>1.73e-08</td>
</tr>
<tr>
<td>00:00:01:241</td>
<td>1.56e-08</td>
<td>8.33e+08</td>
<td>1.30e+01</td>
<td>1.94e-08</td>
<td>4.13e+08</td>
<td>8.00e+00</td>
<td>1.19e-08</td>
</tr>
<tr>
<td>00:00:01:424</td>
<td>1.09e-08</td>
<td>9.16e+08</td>
<td>1.00e+01</td>
<td>1.32e-08</td>
<td>4.54e+08</td>
<td>6.00e+00</td>
<td>8.67e-09</td>
</tr>
</tbody>
</table>

Test Times and Confidence Levels

A true Error Ratio measurement must be statistically valid. Because it is not possible to predict with certainty when errors will occur, your device must be tested long enough to have confidence in its Error Ratio performance.
Calculated Results

The following results are displayed when the bit coded patterns are loaded in **Sequence Editor**:

- **Errored Zeros**: Displays the number of errored zeros during the accumulation period.
- **Errored Ones**: Displays the number of errored ones during the accumulation period.
- **Error Bits**: Displays the number of errored bits during the accumulation period.
- **Compared Zeros**: Displays the number of compared zeros during the accumulation period.
- **Compared Ones**: Displays the number of compared ones during the accumulation period.
- **Compared Bits**: Displays the number of compared bits during the accumulation period.
- **Error Ratio**: Displays the ratio of the number of errors to the number of bits.
- **Error Zero Ratio**: Displays the ratio of the number of error zero to the number of bits.
- **Error One Ratio**: Displays the ratio of the number of errors one to the number of bits.
- **Total Words**: Displays the total number of received sequencer words.
- **Frames**: Displays the number of frames received in a time interval.
- **Errored Frames**: Displays the number of errored frames received in a time interval.
- **Frame Error Ratio**: Displays the ratio of the number of frame errors to the number of frames received in the current (or last completed) accumulation period.
- **ConfidenceLevel@TargetErrorRatio**: Displays the percentage of confidence level achieved at specified target error ratio at certain point of time.
• **ErrorRatio@TargetConfidenceLevel**: Displays the number of error ratio achieved at specified confidence level at certain point of time.

• **Results**: Display the measurement result either *Pass* or *Fail*. It is only available when the “Accumulation End” is selected as “Pass/Fail”.

However, when the symbol coded patterns are loaded in **Sequence Editor**, the following results are displayed:

<table>
<thead>
<tr>
<th>Location</th>
<th>Symbol Error Ratio</th>
<th>Received Symbols</th>
<th>Compared Symbols</th>
<th>Errored Symbols</th>
<th>Illegal Symbol Ratio</th>
<th>Illegal Symbols</th>
<th>Filler Symbol Ratio</th>
<th>Filler Symbols</th>
<th>Disparity Error Ratio</th>
<th>Wrong Disparity</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1.Data11</td>
<td>9.15e-11</td>
<td>2.19e+10</td>
<td>2.19e+10</td>
<td>2.00e+00</td>
<td>0.00e+00</td>
<td>0.00e+00</td>
<td>0.00e+00</td>
<td>1.00e+00</td>
<td>4.50e-11</td>
<td>1.00e+00</td>
</tr>
</tbody>
</table>

• **Symbol Error Ratio**: Displays the symbol ratio of the number of errored symbols to the total number of symbols received.

• **Received Symbols**: Displays the total number of Received Symbol Count (all incoming symbols excluding incoming filler symbols) received in a time interval.

• **Compared Symbols**: Displays the number of compared symbols considered for the accumulation period.

• **Errored Symbols**: Displays the number of errored symbols measured during the accumulation period.

• **Illegal Symbol Ratio**: Displays the ratio of the number of Illegal Symbol count to the number of symbols received in the accumulation period.

• **Illegal Symbols**: Displays the total number of Illegal Symbols received in the accumulation period.

• **Filler Symbols Ratio**: Displays the ratio of total no of filler symbols to the number of symbols received during the accumulation period.

• **Filler Symbols**: Displays the total no of filler symbols received during the accumulation period.

• **Disparity Error Ratio**: Displays the ratio of the number of illegal disparity change count to the number of symbols received in the accumulation period.

• **Wrong Disparity**: Displays the total number of wrong disparity received in the accumulation period.

• **Error Ratio**: Displays the ratio of the number of errors to the number of bits.

• **Compared Bits**: Displays the number of compared bits during the accumulation period.
• **Errored Bits**: Displays the number of errored bits during the accumulation period.

• **ConfidenceLevel@TargetErrorRatio**: Displays the percentage of confidence level achieved at specified target error ratio at certain point of time.

• **Results**: Displays the measurement result either **Pass** or **Fail**. It is only available when the "Accumulation End" is selected as "Pass/Fail".

• **Total Words**: Displays the total number of received sequencer words.

• **Frame Error Ratio**: Displays the ratio of the number of frame errors to the number of frames received in the accumulation period.

• **Frames**: Displays the number of frames received in a time interval.

• **Errored Frames**: Displays the number of errored frames received in a time interval.

• **ErrorRatio@TargetConfidenceLevel**: Displays the number of error ratio achieved at specified confidence level at certain point of time.

The following results are displayed when an **Error Ratio** measurement is performed with PAM4 line coding:

- **Symbol Error Ratio**: Displays the symbol ratio of the number of errored symbols to the total number of symbols received.

- **Errored Symbols**: Displays the number of errored symbols considered for the accumulation period.

- **Compared Symbols**: Displays the number of compared symbols considered for the accumulation period.

- **Error Ratio**: Displays the ratio of the number of errors to the number of bits.

- **Compared Bits**: Displays the number of compared bits during the accumulation period.

- **Errored Bits**: Displays the number of errored bits during the accumulation period.
Error Ratio Measurement for a Group of Analyzers

The error ratio measurement can also be executed on a group of analyzers and combined result will appear in form of Graph, Data Tab and Calculated Results.

To run this, an Accumulation Stop Criteria parameter is available under Acquisition Parameters. It can be set as "Per Analyzer" or "Combined Analyzer".

- **Per Analyzer** - Graph, Data Tab and combined Calculated Results will not be visible.
- **Combined Analyzer** - Graph, Data Tab and combined Calculated Results will be visible.

This parameter will be only be available when a group is selected as an analyzer (if the group is having only one location, this will not be available to the user). Also, the availability of this parameter depends on "Accumulation End" parameter. If the "Accumulation End" is set as "Full Duration", it will not be available. However, the results for group of analyzers will be visible in the Calculated Results.

Follow the given steps to calculate combined results for an analyzer group:

1. Select the analyzer group.
2. Specify Accumulation End as "Pass/Fail" or "Number of Bits".
3. Specify Accumulation Stop Criteria as "Combined Analyzer".
4. Specify Accumulation Duration, Fixed Time and Interval.
5. In case the Accumulation End is selected as Pass/Fail, set Target Error Ratio and Target Confidence Level.
6. In case the Accumulation End is selected as Number of Bits, specify No. of Compared Bits.
7 Run the measurement.
8 The calculated results for the analyzer group will appear as shown in the following figure:
9 Utilities

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Licenses Window / 534
Settings Window / 535
Logger Window / 538
SCPI Server Information / 539
Plug-in Manager / 540
Overview

The M8070B system software provides the following utilities:
- Licenses Window
- Settings Window
- Logger Window
- SCPI Server Information
- Plug-in Manager Window

In addition, the M8070B system software also provides the following utilities will be only available on installing the Advanced Measurement Package plugin:
- Script Editor
- DUT Control Interface
- SCPI Editor
- Self Test Utility

For details, on the utilities provided by Advanced Measurement Package, please refer to M8000 Series Advanced Measurement Package User Guide.

Please note that the Advanced Measurement Package requires license for its activation. For details on license, see M8070B Plugin Licenses on page 560.
Self Test Utility

The **Self Test** utility checks the specific system information of the hardware components for basic functionality. On execution, the following results are displayed:
- System related information such as connected modules, serial no. and hardware revision.
- Module related information such as calibration, power supplies and memory controller.

Launching the Self Test Utility

To launch the **Self Test**:
- Go to the **Menu Bar**  >  **Utilities** and then select **Self Test**.

The **Self Test** utility will appear as shown in the following figure:

![Self Test Utility GUI](image)

The **Self Test** utility consists of the following GUI elements:
- Toolbar
- Self Test History
- Self Test Results Window
Utilities

Toolbar

The toolbar provides the following convenient self test functions:

Table 66

<table>
<thead>
<tr>
<th>Icon</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Execute Self Test" /></td>
<td>Execute Self Test</td>
<td>Click this icon to run the self test.</td>
</tr>
<tr>
<td><img src="image" alt="Abort Self Test" /></td>
<td>Abort Self Test</td>
<td>Click this icon abort a self test.</td>
</tr>
<tr>
<td><img src="image" alt="Save Self Test" /></td>
<td>Save Self Test</td>
<td>Click this icon to save the selected self test from the history. For details, refer to Saving Self Test Results on page 532.</td>
</tr>
<tr>
<td><img src="image" alt="Delete Self Test" /></td>
<td>Delete Self Test</td>
<td>Click this icon to delete the selected self test from the history.</td>
</tr>
<tr>
<td><img src="image" alt="Close Report" /></td>
<td>Close Report</td>
<td>Click this icon to close the self test result.</td>
</tr>
</tbody>
</table>

Self Test History

The Self Test History maintains the history of self tests (Passed or Failed) executed by the user. The passed self test results are indicated by green LED while the failed ones are indicated by red LED.
At any point of time, you can double-click on the shown self test entries to view their respective results. Once viewed, you can click on Close Report icon to close the self test results.

The Self Test History also allows you to save and delete the self test reports. For details, refer to Saving Self Test Results on page 532 and Deleting Self Test Results on page 533.

Self Test Results Window

The Self Test Results window displays the results of the executed self test. It display the following results:

- System related information such as connected modules, serial no. and hardware revision.
- Module related information such as calibration, power supplies and memory controller.

Executing Self Test

To execute a self test:

- Terminate each Data Out port with 50 Ω.
- Remove any devices from the tested M8000 system as any connected device under test might be damaged.
- Click the Execute Self Test icon. The following message will appear:
- Click on **Perform Test** button present on the message box.
- The self test will start and the status will be indicated by the status indicator that appears on the right side of the toolbar. Once the self test is completed, the results will be shown on the **Self Test Results** window.

**CAUTION**

Before performing a system self-test, terminate each **Data Out** port with 50 Ω. Take care to remove any devices from the tested M8000 system as any connected device under test might be damaged.

---

**Aborting Self Test**

To abort a self test:

- Click **Abort Self Test** icon to abort the self test. The self test will stop and the self test failure entry will be displayed in the **Self Test History**.

**Saving Self Test Results**

To save the self test results from the **Self Test History**:

- Click the **Save Report** icon. A standard **Save Result** dialog will appear.
• Use the navigation pane to provide a location to save the file.
• Provide a file name and specify the file format. You can save the file in RTF, HTML, XML and TXT formats.
• Click Save.

Deleting Self Test Results

To delete a self test entry from the **Self Test History**:
• Click **Delete Report** icon. The entry will be removed from the **Self Test History**.
Licenses Window

The **Licenses** window displays the license information currently installed in the modules or host.

Launching the Licenses Window

To launch the **Licenses** window:

1. Go to the **Menu Bar > Utilities** and then select **Licenses...**

   The **Licenses** window is shown in the following figure:

2. Select an option from the **Show Licenses** drop-down list.

   The following options are available:

   - **All**: Displays a list of all the licenses. By default, this option is selected.
   - **Installed**: Displays a list of installed licenses only.
The **Licenses** window is divided into two panels. The left panel shows the modules/host information. Once you select modules/host, the corresponding license information is shown in the right panel.

To exit the **Licenses** window, click the **Close** button.

For detailed information on the M8020A/M8030A licenses, refer to **Licenses** on page 547.

**Settings Window**

The **Settings** window allows you to set the display and channel settings in the GUI. In addition, you can use this dialog to enable/disable **Parameter** hint dialog on the GUI startup.

To open the **Settings** window, go to **Menu Bar > Utilities** and then select **Settings...** The **Setting** window will appear as shown in the following figure:

![Settings Window](image)

The **Settings** window has the following tabs:

- Display tab
- Channel tab
- Hints tab
Utilities

Display Tab

The Display tab provides the following options:

- **Display** - The Display option provides the following choices:
  - **Color Scheme** - Use this option to change the color scheme of the GUI. You can choose between the dark or light scheme. The dark scheme is selected by default.
  - **Font Setting** - Use this option to change the font settings in the GUI.
  - **Use System Fonts** - Select this option to use the system fonts in the GUI.

Keypad Visibility

- **Disable Keypad** - Use this option to disable the on-screen numeric keypad in the GUI. The on-screen numeric keypad is enabled by default.

Channel Tab

- The Channel tab displays the color schemes applied to the various channels of the connected modules. In addition, this tab also allows you to assign your own color schemes to each individual channel of the connected modules.

The following figure depicts how the different color schemes are applied to the various channels of the connected modules.
You can also select **Use Instrument Front Panel Colors** option to assign the color which is available on the front panel of the instrument to each individual channel.

The color schemes assigned to the channels will change if you switch to light color scheme from the **Display Setting** tab.

**NOTE**

Hints Tab

The **Hints** tab allows you to show/hide the **Parameter** hint dialog which appears in the **Setup View** on the GUI startup. For details, see **Setup View** on page 188. Select/unselected the corresponding check-box to show/hide the **Parameter** hint dialog.
Logger Window

The Logger window displays errors, warnings and information messages along with their respective descriptions, applications from where they are generated and their time stamps.

The Logger window always appears whenever you launch the M8070B user interface. However, you can open/close this window by clicking on the Logger button, present on the status bar.

The Logger window allows you to:

- **Message Selection** - Use this option to choose whether you want to view errors, warnings or information message.
- **Copy** - Use this option to copy a message. You need to select a message in order to enable copy feature.
- **Select All** - Use this option to select all messages. It also enables copying all messages.
- **Clear Messages** - Use this option to delete all messages.
- **Auto Scroll** - Use this option to enable/disable auto scroll option. When the Auto Scroll option is enabled, it will automatically scroll you to the new message without using the scroll bar.
- **Open On Message** - Turn this button OFF if you don’t want the Logger window to automatically pop-up whenever a message is received.
- **Column Option** - Use this button to filter the messages either from Log From column or Date and Time column.
- **Search Messages** - Use this option to search messages by providing an input in the Search Messages search box.
SCPI Server Information

This dialog lists the VISA resource and remote access strings to connect instruments.

For Remote Access: Use "CND-181000.msr.is.keysight.com" instead of "localhost".

Note: To use TCP/IP connections it may be necessary to add the instrument in the Keysight Connection Expert.
Plug-in Manager

A plug-in is a piece of software application that acts as an add-on to the main software and enhances its capability. Plug-in allows the software to host additional functionality without undergoing a major modification or enhancement. A plug-in is not a permanent part of the software, hence can be installed, uninstalled and updated as and when required.

The M8070B system software for the M8000 Series of BER Test Solutions supports plug-ins. Thus, the present capabilities of M8070B can be further enhanced by simply adding the required plug-ins.

The Plug-in Manager simplifies all the tasks related to plug-in management. It displays list of plug-ins that are installed in the software. For each plug-in, it displays the information such as Name, Version, Vendor, Description, State and Build Date. In addition, the Plug-in Manager also allows you to install, uninstall and update the plug-ins.

How to Launch Plug-in Manager

To launch Plug-in Manager, open the M8070B user interface and then go to Menu > Utilities and then Plug-in Manager. The Plug-in Manager window will appear as shown in the following figure:

The Plug-in Manager window displays two types of plug-ins:
- **Compatible Plug-ins** – plug-ins which are compatible with the current version of software.
- **In-Compatible Plug-ins** – plug-ins which are not compatible with the current version of software.
The **Plug-in Manager** window displays the following information of each plug-in:

- **Name** - Name of the plug-in
- **Version** - Version no. of the plug-in
- **Vendor** - Vendor/publisher of the plug-in
- **Description** - Brief description of the plug-in
- **State** - State of the plug-in. For details on different plug-in states, see Plug-in States on page 541.
- **Build Date** - Build date of the plug-in

### Plug-in States

There can be the following plug-in states:

- **Installed** - When the plug-in is installed but the M8070B software is not re-started. In this case, the installed plug-in is not loaded or it cannot be used. You have re-start the M8070B software in order to load the plug-in.

- **Loaded** - When the plug-in is installed and the M8070B software has been re-started. In this case, the installed plug-in is ready to be used. Remember, you have to restart the M8070B software in order to load the plug-in.

- **Not Loaded** - When the plug-in is installed and but failed to load. In this case, the installed plug-in cannot be used.

- **Version In-Compatible** - When the version of the installed plug-in is not compatible with the current version of M8070B software.

### How to Install a Plug-in

The **Plug-in Manager** window allows you to install a plug-in.

To do so:

1. Download plug-in file from Keysight webpage: www.keysight.com/find/m8000

2. Click on **Install Plug-in from File** button. A Window’s standard **Open** dialog will appear.

3. Locate the plug-in file (*.M8KP) you want to install and click **OK**.

4. On the successful installation of plug-in, the following message will appear:
Restart the software. Once you restart the software, the plug-in state will change to **Loaded**. See Plug-in States on page 541.

**NOTE**

Ensure to restart the M8070B software for the changes to take effect.

---

**How to Uninstall a Plug-in**

The **Plug-in Manager** window allows you to uninstall a plug-in.

To do so;

1. Select the plug-in from the list.
2. Click on **Uninstall Selected Plug-in** button or right-click on the selected plug-in. The **Uninstall Plug-in** dialog will open.

3. Click **Yes**. If the state of plug-in is **Installed**, then it will be immediately uninstalled from the software.
4. However, if the plug-in is currently in use (**Loaded** or **Not Loaded**), then you will receive the following message.
How to Update a Plug-in

The Plug-in Manager window also allows you to update an already installed plug-in.

Following the given steps to update the plug-in with its higher version:

1. Download plug-in file from Keysight webpage:
   www.keysight.com/find/m8000

2. Click on Install Plug-in from File button. A Window's standard Open dialog will appear.

3. Locate the plug-in file (*.M8KP) you want to update and click OK. You will see the following message:

4. Click Yes. If the state of plug-in is Installed, then it will be immediately updated and the following message will appear:

5. Restart the software. The plug-in will be uninstalled on software startup.
5 However, if the plug-in is currently in use (Loaded or Not Loaded), then you will receive the following message.

6 Click Yes. The following message will appear.

7 Click OK. The selected plug-in will be uninstalled from the software. You can now install the new version of that plug-in. For installation procedure, see How to Install a Plug-in on page 541.
The Plug-in Manager window does not directly allow you to update an installed plug-in with previous (lower) version. If you try to do so it will give the following error message:

```
Installation Failed!

Higher version 3.4.88.1 of MIPI_CPHY_Editor_Plugin is already installed. Installation will not continue.
```

In this case, you have to uninstalled the plug-in and then install the previous (lower) version of that plug-in again.

How to Access an Installed Plug-in Through M8070B User Interface

Follow the steps to access an installed plug-in through M8070B user interface:

1. Launch M8070B software user interface.
2. In the M8070B user interface, go to Menu Bar and then click Application menu. It will list all installed plug-ins.
3. Select the plug-in.
4. The plug-in user interface will appear in the M8070B software.

For complete details on how to operate plug-in user interface, refer to the respective plug-in’s User Guide.

NOTE

Ensure to restart the M8070B software for the changes to take effect.
10 Licenses

Overview / 548
License Types / 549
M8020A/M8030A Licenses / 551
M8040A Licenses / 557
M8070B Plugin Licenses / 560
Keysight License Manager / 563
Installing the Licenses / 566
Overview

The basic functionality of the M8070B can be used without installing any license. However, for advanced operations, you need to install the M8070B plugins. For details on these plugins, see M8070B Supported Plugins on page 68.

In addition, the M8020A, M8030A and M8040A, being a modular product, includes different sets of modules hosted in an M9505A or M9514A AXI chassis, respectively. Each module has its own licenses corresponding to specific features. Therefore, you need to install these licenses in your instrument in order to use these modules/features.

The licenses for the plugins and modules can be installed using the Keysight License Manager. See Keysight License Manager on page 563.
License Types

The Keysight Licensing provides four types of licenses:

- **Node-locked** - A node-locked license permits the licensed software to run on only one machine. Each node-locked license is locked to an instrument or computer. Trial licenses are node-locked, time-based licenses. Trial licenses are issued for a particular instrument or computer and are provided free of charge for you to try out a Keysight product.

A trial license can be of the following two types:

- **30 days free trial license** - The 30 days free trial license for the M8000 Series of BER Test Solutions can be downloaded using the following weblink:
  

- **9 months DST license** - The DST license can only be ordered by rental companies and distributors.

- **USB portable** - A USB portable license is locked to a USB dongle (also called a USB key). Systems that run the licensed feature or product must have the license file resident on their hard disks, and have the dongle attached when they run the licensed feature or product.

Node-locked and USB portable licenses may be counted or uncounted. Counted licenses enable a specified number of a given capability. An uncounted license simply unlocks the licensed feature or application on the system where it is installed.

- **Transportable** - A transportable license is a type of node-locked license that can be unlocked from one client host and then locked to another client host, via a network-enabled process performed in conjunction with the Keysight Software Manager website.

- **Floating** - Floating licenses (network licenses) reside on a license server (a separate computer) and are checked out for use by Keysight products (instruments or applications), then returned (checked in) when no longer needed so that they can be used on another computer or instrument.

Floating licenses can also be borrowed for a specified number of days. Once you have borrowed a license, you can disconnect the licensed instrument or computer from the license server and continue to use the license offline for the duration of the borrow period. Some older floating licenses do not support borrowing.

Each license is either perpetual (permanent) or time-based (good for a limited amount of time).
These licenses can be installed using the Keysight License Manager. It helps you install licenses on your local machine (instrument or computer), or configure your local machine to use licenses from a remote license server. For details, see Keysight License Manager on page 563.

Module-Specific Licenses

Module-specific licenses are a specialized type of license that enables a specific module of a modular instrument (such as a PXI or AXIe module). The module-specific license resides on the controller and is bound to both the controller (typically a PC) and the module; the controller by means of the HostID, and the module itself by means of the module serial number which is embedded in the feature name for the license. Module-specific licenses may be time-perishable.
M8020A/M8030A Licenses

The licenses used by the various modules of M8020A/M8030A are listed in the following tables:

M8041A - High-Performance BERT Module

M8041A - Basic Selection

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8041A-G08</td>
<td>G08</td>
<td>Generator one Channel, Data Rate up to 8.5 Gb/s</td>
</tr>
<tr>
<td>M8041A-G16</td>
<td>G16</td>
<td>Generator one Channel, Data Rate up to 16 Gb/s (Upgrade: U16)</td>
</tr>
<tr>
<td>M8041A-C08</td>
<td>C08</td>
<td>BERT one Channel, Data Rate up to 8.5 Gb/s</td>
</tr>
<tr>
<td>M8041A-C16</td>
<td>C16</td>
<td>BERT one Channel, Data Rate up to 16 Gb/s (Upgrade: UED)</td>
</tr>
</tbody>
</table>

M8041A - Module Functionality

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8041A-0G2</td>
<td>0G2</td>
<td>Second Channel for Generator, License</td>
</tr>
<tr>
<td>M8041A-0A2</td>
<td>0A2</td>
<td>Second Channel for Analyzer, License</td>
</tr>
<tr>
<td>M8041A-0G3</td>
<td>0G3</td>
<td>Advanced Jitter Sources for Receiver Characterization, Module-wide License</td>
</tr>
<tr>
<td>M8041A-0G4</td>
<td>0G4</td>
<td>Multi-tap De-emphasis, Module-wide License</td>
</tr>
<tr>
<td>M8041A-0G5</td>
<td>0G5</td>
<td>Adjustable ISI, Module-wide License</td>
</tr>
<tr>
<td>M8041A-0G6</td>
<td>0G6</td>
<td>Reference Clock Input with Multiplying PLL, Clockgroup-wide License</td>
</tr>
<tr>
<td>M8041A-0G7</td>
<td>0G7</td>
<td>Advanced Interference Sources for Receiver Characterization, Module-wide License</td>
</tr>
<tr>
<td>M8041A-0S1</td>
<td>0S1</td>
<td>Interactive Link Training for PCI Express, Clockgroup-wide License</td>
</tr>
<tr>
<td>M8041A-0S2</td>
<td>0S2</td>
<td>SER/FER Analysis for Coded and Retimed Loopback, Clockgroup-wide License</td>
</tr>
</tbody>
</table>
### M8041A - License Upgrades for M8041A High-Performance BERT Module

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8041A-0A3</td>
<td>0A3</td>
<td>Analyzer Equalization, Module-wide License</td>
</tr>
<tr>
<td>M8041A–0S3</td>
<td>0S3</td>
<td>Interactive Link Training for USB 3.0 and USB 3.1, Module wide License</td>
</tr>
<tr>
<td>M8041A–0S4</td>
<td>0S4</td>
<td>Interactive Link Training for PCI Express for PCI Express 8GT/s and 16GT/s, Clock Group wide License</td>
</tr>
<tr>
<td>M8041A–0S1</td>
<td>0S1</td>
<td>Interactive Link Training for PCI Express, 8GT/s, Clock Group wide License</td>
</tr>
<tr>
<td>M8041A–0SX</td>
<td>0SX</td>
<td>10GBASE-KR Transmitter Equalization Training, Module-wide License</td>
</tr>
</tbody>
</table>

### M8041A - License Upgrades for M8041A High-Performance BERT Module

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8041A-U16</td>
<td>U16</td>
<td>Upgrade to 16 Gb/s data rate from M8041A-G08 and M8041A-C08, Module-wide License</td>
</tr>
<tr>
<td>M8041A-UED</td>
<td>UED</td>
<td>Upgrade to BERT from M8041A-G08 and M8041A-G16, Module-wide License</td>
</tr>
<tr>
<td>M8041A-UG2</td>
<td>UG2</td>
<td>Upgrade to Second Channel for Generator, License</td>
</tr>
<tr>
<td>M8041A-UA2</td>
<td>UA2</td>
<td>Upgrade to Second Channel for Analyzer, License</td>
</tr>
<tr>
<td>M8041A-UG3</td>
<td>UG3</td>
<td>Upgrade to Advanced Jitter Sources for Receiver Characterization, Module-wide License</td>
</tr>
<tr>
<td>M8041A-UG4</td>
<td>UG4</td>
<td>Upgrade to Multi-tap De-emphasis, Module-wide License</td>
</tr>
<tr>
<td>M8041A-UG5</td>
<td>UG5</td>
<td>Upgrade to Adjustable ISI, Module-wide License</td>
</tr>
<tr>
<td>M8041A-UG6</td>
<td>UG6</td>
<td>Upgrade to Reference Clock Input with Multiplying PLL, Clockgroup-wide License</td>
</tr>
<tr>
<td>M8041A-UG7</td>
<td>UG7</td>
<td>Upgrade to Advanced Interference Sources for Receiver Characterization, Module-wide License</td>
</tr>
<tr>
<td>M8041A-US1</td>
<td>US1</td>
<td>Upgrade to Interactive Link Training for PCI Express, Clockgroup-wide License</td>
</tr>
<tr>
<td>M8041A-US2</td>
<td>US2</td>
<td>Upgrade to SER/FER Analysis for Coded and Retimed Loopback, Clockgroup-wide License</td>
</tr>
<tr>
<td>M8041A-UA3</td>
<td>UA3</td>
<td>Upgrade to Analyzer Equalization, Module-wide License</td>
</tr>
<tr>
<td>M8041A-US3</td>
<td>US3</td>
<td>Upgrade to Interactive Link Training for USB 3.0 and USB 3.1, Module wide License</td>
</tr>
<tr>
<td>M8041A-US4</td>
<td>US4</td>
<td>Upgrade to Interactive Link Training for PCI Express for PCI Express 8GT/s and 16GT/s, Clock Group wide License</td>
</tr>
<tr>
<td>M8041A–U14</td>
<td>U14</td>
<td>Upgrade of M8041A-0S1 to 0S4, Interactive Link Training for PCI Express for 8GT/s and 16GT/s, Clock Group wide License</td>
</tr>
</tbody>
</table>
M8051A - High-Performance BERT Module

**M8051A- Basic Selection**

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8041A-US1</td>
<td>US1</td>
<td>Upgrade to Interactive Link Training for PCI Express, 8GT/s, Clock Group wide License</td>
</tr>
<tr>
<td>M8041A-USX</td>
<td>USX</td>
<td>Upgrade to 10GBASE-KR Transmitter Equalization Training, Module-wide License</td>
</tr>
<tr>
<td>M8041A-UR3</td>
<td>UR3</td>
<td>Upgrade of M8041A-0A3 with latest CTE Presets, Return-to-Factory</td>
</tr>
</tbody>
</table>

**M8051A- Module Functionality**

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8051A-G08</td>
<td>G08</td>
<td>Generator one Channel, Data Rate up to 8.5 Gb/s</td>
</tr>
<tr>
<td>M8051A-G16</td>
<td>G16</td>
<td>Generator one Channel, Data Rate up to 16 Gb/s (Upgrade: U16)</td>
</tr>
<tr>
<td>M8051A-C08</td>
<td>C08</td>
<td>BERT one Channel, Data Rate up to 8.5 Gb/s</td>
</tr>
<tr>
<td>M8051A-C16</td>
<td>C16</td>
<td>BERT one Channel, Data Rate up to 16 Gb/s (Upgrade: UED)</td>
</tr>
</tbody>
</table>
### M8051A - License Upgrades for M8051A High-Performance BERT Module

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8051A-0G7</td>
<td>G7</td>
<td>Advanced Interference Sources for Receiver Characterization, Module-wide License</td>
</tr>
<tr>
<td>M8051A-0A3</td>
<td>A3</td>
<td>Analyzer Equalization, Module-wide License</td>
</tr>
<tr>
<td>M8051A-0SX</td>
<td>SX</td>
<td>10GBase-KR Transmitter Equalization Training, module-wide license</td>
</tr>
<tr>
<td>M8051A-U16</td>
<td>U16</td>
<td>Upgrade to 16 Gb/s data rate from M8051A-G08 and M8051A-C08, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UED</td>
<td>UED</td>
<td>Upgrade to BERT from M8051A-G08 and M8051A-G16, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UG2</td>
<td>UG2</td>
<td>Upgrade to Second Channel for Generator, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UA2</td>
<td>UA2</td>
<td>Upgrade to Second Channel for Analyzer, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UG3</td>
<td>UG3</td>
<td>Upgrade to Advanced Jitter Sources for Receiver Characterization, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UG4</td>
<td>UG4</td>
<td>Upgrade to Multi-tap De-emphasis, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UG5</td>
<td>UG5</td>
<td>Upgrade to Adjustable ISI, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UG7</td>
<td>UG7</td>
<td>Upgrade to Advanced Interference Sources for Receiver Characterization, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UA3</td>
<td>UA3</td>
<td>Upgrade to Analyzer Equalization, Module-wide License</td>
</tr>
<tr>
<td>M8051A-U16</td>
<td>U16</td>
<td>Upgrade to 16 Gb/s data rate from M8051A-G08 and M8051A-C08, Module-wide License</td>
</tr>
<tr>
<td>M8051A-USX</td>
<td>USX</td>
<td>Upgrade to 10GBase-KR Transmitter Equalization Training, Module-wide License</td>
</tr>
<tr>
<td>M8051A-UR3</td>
<td>UR3</td>
<td>Upgrade of M8051A-0A3 with latest CTLE Presets, Return-to-Factory</td>
</tr>
<tr>
<td>M8051A-US6</td>
<td>US6</td>
<td>Upgrade to SAS-3 transmitter equalization training, module-wide license</td>
</tr>
</tbody>
</table>
### M8061A Multiplexer 2:1 with De-emphasis

**Table 73  M8061A Licenses**

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8061A-001</td>
<td>001</td>
<td>32 Gb/s multiplexer</td>
</tr>
<tr>
<td>M8061A-004</td>
<td>004</td>
<td>4-tap de-emphasis</td>
</tr>
<tr>
<td>M8061A-008</td>
<td>008</td>
<td>Extension to 8-tap de-emphasis</td>
</tr>
<tr>
<td>M8061A-U04</td>
<td>U04</td>
<td>Upgrade to 4-tap de-emphasis</td>
</tr>
<tr>
<td>M8061A-U08</td>
<td>U08</td>
<td>Upgrade to 8-tap de-emphasis</td>
</tr>
</tbody>
</table>

### M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

**Table 74  M8062A - Basic Selection**

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8062A-C32</td>
<td>C32</td>
<td>32 Gb/s BERT front-end</td>
</tr>
<tr>
<td>M8062A-G32</td>
<td>G32</td>
<td>32 Gb/s Pattern generator front-end</td>
</tr>
</tbody>
</table>
M8062A - Module Functionality

Table 75  M8062A - Module Functionality

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8062A-0G4</td>
<td>0G4</td>
<td>Multi-tap De-emphasis License</td>
</tr>
<tr>
<td>M8062A-0G5</td>
<td>0G5</td>
<td>Adjustable Intersymbol Interference (ISI) License</td>
</tr>
<tr>
<td>M8062A-0A3</td>
<td>0A3</td>
<td>Analyzer Equalization License</td>
</tr>
<tr>
<td>M8062A-0A4</td>
<td>0A4</td>
<td>Clock Recovery up to 32 Gb/s</td>
</tr>
<tr>
<td>M8062A-OSC</td>
<td>OSC</td>
<td>100BASE-KR4 and 25GBASE-KR Transmitter Equalization Training, Module-wide License</td>
</tr>
</tbody>
</table>

M8062A - License Upgrades for M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

Table 76  M8062A - License Upgrades for M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8062A-UED</td>
<td>UED</td>
<td>Upgrade of M8062A-G32 Pattern Generator to M8062A-C32 BERT License</td>
</tr>
<tr>
<td>M8062A-UA3</td>
<td>UA3</td>
<td>Upgrade of M8062A to Analyzer Equalization License</td>
</tr>
<tr>
<td>M8062A-UG4</td>
<td>UG4</td>
<td>Upgrade of M8062A to Multi-tap De-emphasis License</td>
</tr>
<tr>
<td>M8062A-UG5</td>
<td>UG5</td>
<td>Upgrade of M8062A to Adjustable Intersymbol Interference License</td>
</tr>
<tr>
<td>M8062A-UA4</td>
<td>UA4</td>
<td>Upgrade of M8062A to Clock Recovery up to 32 Gb/s</td>
</tr>
<tr>
<td>M8062A-USC</td>
<td>USC</td>
<td>Upgrade of 100BASE-KR4 and 25GBASE-KR Transmitter Equalization Training, module-wide license</td>
</tr>
<tr>
<td>M8062A-US6</td>
<td>US6</td>
<td>Upgrade to SAS-3 transmitter equalization training, module-wide license</td>
</tr>
</tbody>
</table>

**NOTE**

In addition to the M8062A-UA4 license, M8062A modules with serial numbers < MY55400300 may also require a hardware upgrade in order to enable the CDR feature.
## M8045A Licenses

**M8045A Pattern generator and clock module, 32/64 Gbaud**

### M8045A - Basic Selection

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8045A-G32</td>
<td>G32</td>
<td>Pattern generator one channel NRZ, data rate up to 32 Gbaud (requires remote head, M8057A/B)</td>
</tr>
<tr>
<td>M8045A-G64</td>
<td>G64</td>
<td>Pattern generator one channel NRZ, data rate up to 64 Gbaud (requires remote head, M8057A/B)</td>
</tr>
<tr>
<td>M8045A-0G2</td>
<td>0G2</td>
<td>Second channel, hardware and license (requires remote head, M8057A/B)</td>
</tr>
<tr>
<td>M8045A-0G3</td>
<td>0G3</td>
<td>Advanced jitter sources for receiver characterization, module-wide license</td>
</tr>
<tr>
<td>M8045A-0G4</td>
<td>0G4</td>
<td>De-emphasis, module-wide license</td>
</tr>
<tr>
<td>M8045A-0P3</td>
<td>0P3</td>
<td>PAM4 encoding up to 32 Gbaud, module-wide license</td>
</tr>
<tr>
<td>M8045A-0P6</td>
<td>0P6</td>
<td>Extension to PAM4 encoding up to 64 Gbaud, module-wide license</td>
</tr>
<tr>
<td>M8045A-0G9</td>
<td>0G9</td>
<td>FEC encoding, module-wide license</td>
</tr>
<tr>
<td>M8045A-0G6</td>
<td>0G6</td>
<td>Reference Clock Input with Multiplying PLL</td>
</tr>
</tbody>
</table>

### M8045A - License Upgrades for M8045A

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8045A-U64</td>
<td>U64</td>
<td>Upgrade to 64 Gbaud (requires remote head, M8057A/B)</td>
</tr>
<tr>
<td>M8045A-UG2</td>
<td>UG2</td>
<td>Upgrade to second channel, hardware and license (requires remote head, M8057A/B)</td>
</tr>
<tr>
<td>M8045A-UG3</td>
<td>UG3</td>
<td>Upgrade to advanced jitter sources for receiver characterization, module-wide license</td>
</tr>
<tr>
<td>M8045A-UG4</td>
<td>UG4</td>
<td>Upgrade to de-emphasis, module-wide license</td>
</tr>
<tr>
<td>M8045A-UP3</td>
<td>UP3</td>
<td>Upgrade to PAM4 encoding up to 32 Gbaud, module-wide license</td>
</tr>
</tbody>
</table>
### Licenses

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8045A-UP6</td>
<td>UP6</td>
<td>Upgrade to extension to PAM4 encoding up to 64 Gbaud, module-wide license</td>
</tr>
<tr>
<td>M8045A-UG9</td>
<td>UG9</td>
<td>Upgrade to FEC encoding</td>
</tr>
<tr>
<td>M8045A-UG6</td>
<td>UG6</td>
<td>Upgrade to reference clock input with multiplying PLL</td>
</tr>
</tbody>
</table>

**NOTE**

Please note that M8045A-UG2 (upgrade to second channel) is a return-to-factory upgrade.

---

**M8046A Analyzer Module, 32/64 Gbaud**

**Table 79**

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8046A-A32</td>
<td>A32</td>
<td>Analyzer, one channel, data rate up to 32 Gbaud, NRZ</td>
</tr>
<tr>
<td>M8046A-A64</td>
<td>A64</td>
<td>Analyzer, one channel, data rate up to 64 Gbaud, NRZ</td>
</tr>
<tr>
<td>M8046A-0P3</td>
<td>0P3</td>
<td>PAM4 decoding up to 32 Gbaud, license</td>
</tr>
<tr>
<td>M8046A-0P6</td>
<td>0P6</td>
<td>PAM4 Extension up to 58 Gbaud, License (requires M8046A with S/N &gt; XXXX2000)</td>
</tr>
<tr>
<td>M8046A-A03</td>
<td>A03</td>
<td>Equalizer license</td>
</tr>
<tr>
<td>M8046A-0A3</td>
<td>0A3</td>
<td>Equalization, license (only needed for &gt; 32 Gbaud)</td>
</tr>
<tr>
<td>M8046A-0A4</td>
<td>0A4</td>
<td>Clock Recovery for 32 Gbaud</td>
</tr>
<tr>
<td>M8046A-0A5</td>
<td>0A5</td>
<td>Clock Recovery for 64 Gbaud</td>
</tr>
<tr>
<td>M8046A-0S1</td>
<td>0S1</td>
<td>Interactive Link Training for PCIe 8/16/32 GT/s</td>
</tr>
<tr>
<td>M8046A-0S2</td>
<td>0S2</td>
<td>SKP OS Filtering for PCIe 8/16/32 GT/s and CCIX 20/25 Gb/s</td>
</tr>
<tr>
<td>M8046A-0S4</td>
<td>0S4</td>
<td>SKP OS Filtering for USB 3.0 and USB 3.1</td>
</tr>
<tr>
<td>M8046A-0S6</td>
<td>0S6</td>
<td>SKP OS Filtering for SATA3, SAS2, and SAS3</td>
</tr>
</tbody>
</table>
## M8046A - License Upgrades for M8046A

<table>
<thead>
<tr>
<th>Product</th>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8046A-UP3</td>
<td>UP3</td>
<td>Upgrade to PAM4 decoding up to 32 Gbaud, license</td>
</tr>
<tr>
<td>M8046A-UP6</td>
<td>UP6</td>
<td>Upgrade of M8046A to PAM4 Extension up to 58 Gbaud, License (requires M8046A-A64, -A3 or -U64, -UA3)</td>
</tr>
<tr>
<td>M8046A-US1</td>
<td>US1</td>
<td>Upgrade to Interactive Link Training for PCIe 8/16/32 GT/s</td>
</tr>
<tr>
<td>M8046A-US2</td>
<td>US2</td>
<td>Upgrade to SKP OS Filtering for PCIe 8/16/32 GT/s and CCIX 20/25 Gb/s</td>
</tr>
<tr>
<td>M8046A-US4</td>
<td>US4</td>
<td>Upgrade to SKP OS Filtering for USB 3.0 and USB3 3.1</td>
</tr>
<tr>
<td>M8046A-US6</td>
<td>US6</td>
<td>Upgrade to SKP OS Filtering for SATA3, SAS2, and SAS3</td>
</tr>
</tbody>
</table>
M8070B Plugin Licenses

### Advanced Measurement Package Licenses

Table 81 on page -560 shows the various licenses available for **Advanced Measurement Package Licenses**:

<table>
<thead>
<tr>
<th>License</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8070ADVB-1FP</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked perpetual license</td>
</tr>
<tr>
<td>M8070ADVB-1TP</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable perpetual license</td>
</tr>
<tr>
<td>M8070ADVB-1NP</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, floating perpetual license</td>
</tr>
<tr>
<td>M8070ADVB-1UP</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable perpetual license</td>
</tr>
<tr>
<td>M8070ADVB-1FL</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked 12 month license</td>
</tr>
<tr>
<td>M8070ADVB-1TL</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 12 month license</td>
</tr>
<tr>
<td>M8070ADVB-1NL</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 12 month license</td>
</tr>
<tr>
<td>M8070ADVB-1UL</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 12 month license</td>
</tr>
<tr>
<td>M8070ADVB-1FX</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked 24 month license</td>
</tr>
<tr>
<td>M8070ADVB-1TX</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 24 month license</td>
</tr>
<tr>
<td>M8070ADVB-1NX</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 24 month license</td>
</tr>
<tr>
<td>M8070ADVB-1UX</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 24 month license</td>
</tr>
<tr>
<td>M8070ADVB-1FY</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked 36 month license</td>
</tr>
<tr>
<td>M8070ADVB-1TY</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 36 month license</td>
</tr>
<tr>
<td>M8070ADVB-1NY</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 36 month license</td>
</tr>
<tr>
<td>M8070ADVB-1UY</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 36 month license</td>
</tr>
<tr>
<td>M8070ADVB-1FF</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked 6 month license</td>
</tr>
<tr>
<td>M8070ADVB-1TF</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 6 month license</td>
</tr>
</tbody>
</table>
Table 82 on page 561 shows the various licenses available for **Error Distribution Analysis Package**:

<table>
<thead>
<tr>
<th>License</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8070ADVB-1NF</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 6 month license</td>
</tr>
<tr>
<td>M8070ADVB-1UF</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 6 month license</td>
</tr>
<tr>
<td>M8070ADVB-TRL</td>
<td>Advanced Measurement Package for M8000 Series BERT Test Solutions, 30 days free Trial</td>
</tr>
<tr>
<td>M8070EDAB-1FP</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked perpetual license</td>
</tr>
<tr>
<td>M8070EDAB-1TP</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable perpetual license</td>
</tr>
<tr>
<td>M8070EDAB-1NP</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating perpetual license</td>
</tr>
<tr>
<td>M8070EDAB-1UP</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable perpetual license</td>
</tr>
<tr>
<td>M8070EDAB-1FL</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked 12 month license</td>
</tr>
<tr>
<td>M8070EDAB-1TL</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 12 month license</td>
</tr>
<tr>
<td>M8070EDAB-1NL</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 12 month license</td>
</tr>
<tr>
<td>M8070EDAB-1UL</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 12 month license</td>
</tr>
<tr>
<td>M8070EDAB-1FX</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked 24 month license</td>
</tr>
<tr>
<td>M8070EDAB-1TX</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 24 month license</td>
</tr>
<tr>
<td>M8070EDAB-1NX</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 24 month license</td>
</tr>
<tr>
<td>M8070EDAB-1UX</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 24 month license</td>
</tr>
<tr>
<td>M8070EDAB-1FY</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked 36 month license</td>
</tr>
<tr>
<td>M8070EDAB-1TY</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 36 month license</td>
</tr>
<tr>
<td>M8070EDAB-1NY</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 36 month license</td>
</tr>
<tr>
<td>M8070EDAB-1UY</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 36 month license</td>
</tr>
<tr>
<td>M8070EDAB-1FF</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked 6 month license</td>
</tr>
<tr>
<td>License Code</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------</td>
<td>------------------------------------------------------------------</td>
</tr>
<tr>
<td>M8070EDAB-1TF</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 6 month license</td>
</tr>
<tr>
<td>M8070EDAB-1NF</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 6 month license</td>
</tr>
<tr>
<td>M8070EDAB-1UF</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 6 month license</td>
</tr>
<tr>
<td>M8070EDAB-TRL</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, 30 days free Trial</td>
</tr>
<tr>
<td>M8070EDAB-DST</td>
<td>Error Distribution Analysis Package for M8000 Series BERT Test Solutions, 9 months TBL</td>
</tr>
</tbody>
</table>
Keysight License Manager

*Keysight License Manager* is a software utility that enables end users to easily manage right-to-use licenses for software and hardware capabilities on Keysight instruments or systems. The graphical user interface (GUI) gives you a visual representation of the licenses installed on your Keysight Technologies systems and provides access to the following features:

- View the licenses installed on a system
- Install licenses for new capabilities
- Transport licenses from one controller to another
- Borrow the licenses
- Remove licenses for capabilities no longer needed

For detailed information on *Keysight License Manager*, refer to the *Keysight License Manager Help*. You can access the *Keysight License Manager Help* from the *Keysight License Manager* web page:

http://www.keysight.com/find/LicenseManager

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**NOTE**

Please note that the Keysight License Manager 6 and Keysight License Manager 5 are installed on your system when you install M8070B system software.

---

There are two versions of Keysight License Manager, which can be used to manage the licenses:

**Keysight License Manager 6**

This license management application allows you to manage floating and USB portable licenses for a variety of software products and instruments.
You can use the Keysight License Manager 6 to configure remote license servers for sharing licenses across a network, or to configure a local license server (used with certain types of node-locked licenses) on the computer or instrument where your Keysight software is installed.

Although, the Keysight License Manager 6 is installed on your system when you install the M8070B software, however, you can download the it at: Keysight License Manager 6

<table>
<thead>
<tr>
<th>USB portable licenses:</th>
<th>Install, view, delete</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floating licenses:</td>
<td>Install, view, delete, borrow, and configure license server</td>
</tr>
</tbody>
</table>

This license management application allows you to manage node-locked and transportable licenses for a variety of software products and instruments.
Although, the Keysight License Manager 5 is installed on your system when you install the M8070B software, however, you can download it at: Keysight License Manager 5
Installing the Licenses

Adding License using Keysight License Manager 6

Adding a Floating License

1. On the license server machine, start Keysight License Manager 6 from your computer's Start screen or Start menu.
2. Click Add a license to your local machine.
3. Select Add a license to this floating license server.
4. In the Add (install) a license window, click Browse... and browse to the location of your license file. You can repeat this as many times as needed to install all your licenses.
5. If you want the license server process to start automatically each time the server machine is restarted, make sure that Automatically start license server after every reboot is selected.

For more information, you can also refer the Keysight Licensing Administrator's Guide:

Specify remote license servers

To tell your Keysight product where to get its floating (network) licenses, do the following.

1. From the Keysight License Manager 6 home screen, click Specify remote license server(s).
2. If you did not run License Manager from a menu in a Keysight product, you will see a product selection dialog box. Select the product to be licensed from the drop-down list.
3. In the License Setup Wizard for <Product Name> dialog box, type in the port_number@host_name of each server. If you have more than one server, separate them with semicolons (;). For example:
4 Once you've entered your server name(s), click **Next** to complete your setup.

**Adding a USB License**

Before adding a USB license, you must ensure that:

- Your Keysight product software is installed on this machine.
- You have a license file on this machine. If you don't have a license file, go to **Keysight Software Manager** to get one.
- If your license is locked to a dongle (USB key) rather than to a host ID:
  - The dongle driver is installed on this machine. To install:
    - Run Setup64.exe and accept the defaults.
    - Get the FLEXID10 USB Dongle Driver from [http://www.keysight.com/find/LicensingUsbDriver](http://www.keysight.com/find/LicensingUsbDriver).
    - Extract the .zip file to this machine.
  - The dongle is connected to a USB port on this machine.

To license a Keysight product for use on this machine, select the product from the drop-down menu. Once you have selected your product, browse to the license file, then click **Next** to add the license.

Counted node-locked or USB portable licenses require a license server process: your local machine is both server and client for this license type. If your local machine was not already running a license server process, that process will be started when you click **Next** to complete the operation. To make sure the server process starts automatically each time you reboot the machine, ensure that **Automatically start license server after every reboot** is selected.

For more information, you can also refer the **Keysight Licensing Administrator's Guide**:
Adding License using Keysight License Manager 5

Adding a Node-Locked License

You can add a license to your system by installing a license (*.lic) file if you receive one from Keysight.

1. Select the Install License File... menu option. This displays a Windows file selection window.
2. Use the file window to browse to and select the license file (<filename>.lic) that you want to add.
3. Click Open. License Manager automatically installs the license file in the folder and notifies you with a pop-up that the license has been stored in your license directory. The license now appears on the main license view.

For more information, you can also refer the Keysight Licensing Administrator's Guide:

Transporting a License

Transportable licenses are licenses that can be moved from one host controller to another using the Keysight License Manager.

1. Start the Keysight License Manager by double clicking the Keysight License Notifier icon or click Start > (All) Programs > Keysight License Manager > Keysight License Manager.
2. In the Keysight License Manager, click on Help > Keysight License Manager Help and perform the procedure in the Transporting Licenses help topic.

Installing Temporary License (Trial License)

A temporary (trial) license can be of the following two types:

• **30 days free trial license** – The 30 days free trial license for the M8000 Series of BER Test Solutions can be downloaded using the following weblink:
Licenses

- **9 months DST license** - The DST license can only be ordered by rental companies and distributors.

The following procedure shows how to redeem and install a trial license on a dedicated host computer.

1. Locate the **Software License Entitlement Certificate**.
2. Follow the instructions on the **Software License Entitlement Certificate** to redeem your license.
3. You will receive a license file (in an email). The file has the suffix .lic.
4. Follow the instructions in the email to complete the installation of the license file.
5. In the M8070B software interface, verify that the license has been installed by selecting **Utilities > Licenses**... then viewing the license status in the **Installed** column.

Installing Module Licenses (not required for M8020A-BU1, M8030A-BU1 and M8040A-BU1)

Module licenses enable specific features in the modules of the M8020A/M8030A/M8040A system. Once a module license has been installed using the **Keysight License Manager**, the next time the M8070B software and M8020A/M8030A/M8040A hardware are started, the license is recognized by the M8070B software and compared to the module’s serial number. If the PC Host ID and serial number match, the EEPROM in the module is programmed and the feature is enabled. Even if the M8070B software license is transported to another host computer, the module feature will remain enabled.

The following procedure shows how to redeem and install a module license.

1. Locate the **Software License Entitlement Certificate**.
2. Follow the instructions on the **Software License Entitlement Certificate** to redeem your license.
3. You will receive a license file (in an email). The file has the suffix .lic.
4. Follow the instructions in the email to complete the installation of the license file.
5. In the M8070B software interface, verify that the license has been installed by selecting **Help > Licenses** then viewing the license status in the **Installed** column.
Appendix

Basic Troubleshooting / 572
M8070B Factory Patterns / 573
Basic Troubleshooting

Updating software components

Updated versions of the M8020A, M8030A, M8040A and module specific software components are available on the Keysight website.

These software components are available as .EXE files. To download a software upgrade:

2. Click the Technical Support tab.
3. Click Drivers and Software.
4. Type the model number of the instrument module for which software update is needed and click Find. Model number is located on the front panel of the module.
5. Click the Driver & Software link on the module page.
6. Download the required software update from the list of available updates.

The chassis does not power up

If the chassis or a module does not appear to power up, check the following:

• The circuit breakers at the rear of the chassis are set to the right, which is the ON position.
• The AC power cords are connected to a working power source.
• The electrical circuits are not overloaded. Check the combined power requirements of all equipment on the same circuit.
• There are no empty slots in the chassis. Leaving slots empty can overheat the inserted modules, causing them to shut down.

Module is exceptionally hot

• Check that the vent holes on the chassis are not blocked.
• Check that a filler panel module or an instrument module is installed into empty slots on either side of an instrument module.

Contacting Keysight Technologies

To locate a sales or service office near you, go to www.keysight.com/find/contactus.
M8070B Factory Patterns

The M8070B System Software provides a set of example factory supplied standard patterns. These patterns mimic real data packets and standard stress patterns.

**NOTE**
Please note that these patterns are read only and cannot be modified. However, if you modify these patterns, you will have to save them with different name at different location.

### CEI

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEIstress_bit</td>
<td>CEI Stress pattern</td>
</tr>
<tr>
<td>CID_bit</td>
<td></td>
</tr>
<tr>
<td>QPRBS13-CEI_bit</td>
<td>This QPRBS13-CEI pattern is defined by OIF CEI-56G VSR Chapter 16.C.3.1 Draft 13. The quaternary PRBS13 test pattern is a 4-level pattern created by encoding a repeating PRBS13 pattern using Gray code and PAM4 encoding. Each cycle of QPRBS13-CEI is 8191 symbols long. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
<tr>
<td>SSPR_bit</td>
<td></td>
</tr>
<tr>
<td>SSPS-16_bit</td>
<td></td>
</tr>
<tr>
<td>SSPS-64_bit</td>
<td></td>
</tr>
</tbody>
</table>

### DisplayPort

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D24.3_b8b10</td>
<td>contains D24.3 symbols; pattern type is B8B10</td>
</tr>
<tr>
<td>DP-TS1_D10.2_b8b10</td>
<td>part of trainings sequence; pattern type is B8B10</td>
</tr>
<tr>
<td>DP-TS2_b8b10</td>
<td>part of trainings sequence; pattern type is B8B10</td>
</tr>
<tr>
<td>HBR2_SR-BF-BF-SR-256_CompEyePattren_b8b10</td>
<td>DP test pattern, see file name for details; pattern type is B8B10</td>
</tr>
<tr>
<td>HBR2_SR-BF-BF-SR-7796_CompEyePattren_b8b10</td>
<td>DP test pattern, see file name for details; pattern type is B8B10</td>
</tr>
</tbody>
</table>
### HBR2_SR-BS-BS-SR-256_CompEyePattern_b8b10
- DP test pattern; see file name for details; pattern type is B8B10

### HBR2_SR-CP-CP-SR-256_CompEyePattern_b8b10
- DP test pattern; see file name for details; pattern type is B8B10

### TPS3_b8b10
- Part of trainings sequence; pattern type is B8B10

### JBERT_CP2520.prtm
- DP test pattern

### JBERT_TPS3
- Part of trainings sequence; pattern type is B8B10

### JBERT_TPS4.prtm
- Part of trainings sequence; pattern type is B8B10

---

### EAQuickStartGuide

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>burst_25_bit</td>
<td>Burst length 25</td>
</tr>
<tr>
<td>burst_25B_bit</td>
<td>Burst length 25</td>
</tr>
<tr>
<td>sensitive_7_bit</td>
<td></td>
</tr>
<tr>
<td>sensitive_7B_bit</td>
<td></td>
</tr>
</tbody>
</table>

---

### FDDI

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDDI_Jitter_bit</td>
<td>The Fiber Distributed Data Interface (FDDI) data dependent jitter test pattern is used for testing FDDI components or physical links. The pattern is 1280 bits long and is transmitted continuously during the test by repeating the pattern. The sequence causes a near worst case condition for inter-symbol interference and duty-cycle, baseline wander.</td>
</tr>
<tr>
<td>FDDI_Wander_bit</td>
<td>The FDDI baseline wander test pattern is used to test FDDI components for the effects of a change in the average DC level of the signal. The first 45,000 bits are of the code group (010101); the last 45,000 bits are of the code group (10101).</td>
</tr>
<tr>
<td>FDDI_Wander_b8b10</td>
<td>The Fiber Distributed Data Interface (FDDI) data dependent jitter test pattern is used for testing FDDI components or physical links.</td>
</tr>
</tbody>
</table>
## FiberChannel/Gigabit Ethernet

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CJTPAT_b8b10</td>
<td>This Fiber Channel Compliant (JTPAT) pattern for jitter tolerance is packaged into a Fiber Channel frame.</td>
</tr>
<tr>
<td>CJTPAT_bit</td>
<td>This Fiber Channel Compliant (JTPAT) pattern for jitter tolerance is packaged into a Fiber Channel frame.</td>
</tr>
<tr>
<td>CRPAT_b8b10</td>
<td>This Fiber Channel Compliant (RPAT) pattern for jitter generation is packaged into a Fiber Channel frame.</td>
</tr>
<tr>
<td>CRPAT_bit</td>
<td>This Fiber Channel Compliant (RPAT) pattern for jitter generation is packaged into a Fiber Channel frame.</td>
</tr>
<tr>
<td>CSPAT_b8b10</td>
<td>This Fiber Channel supply noise (SPAT) pattern is packaged into a Fiber Channel frame for use in system level tests.</td>
</tr>
<tr>
<td>CSPAT_bit</td>
<td>This Fiber Channel supply noise (SPAT) pattern is packaged into a Fiber Channel frame for use in system level tests.</td>
</tr>
<tr>
<td>D21-5_bit</td>
<td>This pattern is used to test Fiber Channel and Gigabit Ethernet elements. It tests random jitter (RJ) and the symmetry of logic transitions. The pattern is composed of alternating logic highs and lows and is repeated continuously. Disparity rules are followed. 1010101010 1010101010 (binary).</td>
</tr>
<tr>
<td>JSPAT_b8b10</td>
<td>This Fiber Channel Compliant (JSPAT) pattern unframed using B8B10 format</td>
</tr>
<tr>
<td>JSPAT_bit</td>
<td>This Fiber Channel Compliant (JSPAT) pattern unframed using BIT format</td>
</tr>
<tr>
<td>JTPAT_b8b10</td>
<td>This is a Fiber Channel jitter tolerance pattern, used to test receiver CDR to large instantaneous phase jumps.</td>
</tr>
<tr>
<td>JTPAT_bit</td>
<td>This is a Fiber Channel jitter tolerance pattern, used to test receiver CDR to large instantaneous phase jumps.</td>
</tr>
<tr>
<td>JTSPAT_b8b10</td>
<td>This Fiber Channel Compliant (JTSPAT) pattern unframed using B8B10 format</td>
</tr>
<tr>
<td>JTSPAT_bit</td>
<td>This Fiber Channel Compliant (JTSPAT) pattern unframed using BIT format</td>
</tr>
<tr>
<td>K28-5_b8b10</td>
<td>K28.5 pattern, tests random and deterministic jitter.</td>
</tr>
<tr>
<td>K28-5_bit</td>
<td>K28.5 pattern, tests random and deterministic jitter.</td>
</tr>
<tr>
<td>K28-7_bit</td>
<td>This pattern is used to test Fiber Channel and Gigabit Ethernet elements. It has a large low frequency content that is used to test low frequency random jitter (RJ) and PLL tracking errors. The pattern is composed of five logic highs, followed by five logic lows. This is repeated continuously and disparity rules are followed: 11111 00000 11111 00000 (binary).</td>
</tr>
<tr>
<td>RPAT_b8b10</td>
<td>This is a Fiber Channel random data pattern.</td>
</tr>
<tr>
<td>RPAT_bit</td>
<td>This is a Fiber Channel random data pattern.</td>
</tr>
<tr>
<td>SPAT_b8b10</td>
<td>This is a Fiber Channel supply noise stimulus test pattern.</td>
</tr>
<tr>
<td>SPAT_bit</td>
<td>This is a Fiber Channel supply noise stimulus test pattern.</td>
</tr>
</tbody>
</table>
## PCI Express

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>compliance_b8b10</td>
<td>Compliance patterns</td>
</tr>
<tr>
<td>compliance_bit</td>
<td>Compliance patterns</td>
</tr>
<tr>
<td>test_payload_b8b10</td>
<td>Compliance pattern; pattern format B8B10</td>
</tr>
<tr>
<td>test_payload_bit</td>
<td>Compliance pattern; pattern format BIT</td>
</tr>
<tr>
<td>ts1_b8b10</td>
<td>part of trainings sequence; pattern format B8B10</td>
</tr>
<tr>
<td>ts1_bit</td>
<td>part of trainings sequence; pattern format BIT</td>
</tr>
<tr>
<td>ts1_skp1_b8b10</td>
<td>part of trainings sequence; pattern format B8B10</td>
</tr>
<tr>
<td>ts1_skp1_bit</td>
<td>part of trainings sequence; pattern format BIT</td>
</tr>
<tr>
<td>ts1_skp_bit</td>
<td>part of trainings sequence; pattern format BIT</td>
</tr>
<tr>
<td>ts2_b8b10</td>
<td>part of trainings sequence; pattern format B8B10</td>
</tr>
<tr>
<td>ts2_bit</td>
<td>part of trainings sequence; pattern format BIT</td>
</tr>
<tr>
<td>ts2_skp_bit</td>
<td>part of trainings sequence; pattern format BIT</td>
</tr>
<tr>
<td>ts2_skp2_b8b10</td>
<td>part of trainings sequence; pattern format B8B10</td>
</tr>
<tr>
<td>ts2_skp2_bit</td>
<td>part of trainings sequence; pattern format BIT</td>
</tr>
</tbody>
</table>

## PCI Express 2

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compliance5G_b8b10</td>
<td></td>
</tr>
<tr>
<td>PCIe2_Compliance_b8b10</td>
<td></td>
</tr>
<tr>
<td>PCIe2_trainLB_1_bit</td>
<td></td>
</tr>
<tr>
<td>PCIe2_trainLB_2_bit</td>
<td></td>
</tr>
<tr>
<td>PCIe2_trainLB_3_bit</td>
<td></td>
</tr>
<tr>
<td>TrainLoopback5G_1_bit</td>
<td></td>
</tr>
<tr>
<td>TrainLoopback5G_2_bit</td>
<td></td>
</tr>
</tbody>
</table>
### PCI Express 3

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calibration/DMSI_CMSI_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/PCIe3_Compliance_lane0_BIT_8G</td>
<td></td>
</tr>
<tr>
<td>Calibration/RJ_SJ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/Step_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/TxEQ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Test/PCIe3_modified_compliance_lane_0_CC_BIT_8G</td>
<td>PCIe 8 GT/s Modified Compliance pattern for lane 0 for common reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/PCIe3_modified_compliance_lane_0_IR_BIT_8G</td>
<td>PCIe 8 GT/s Modified Compliance pattern for lane 0 for independent reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/PCIe3_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_8G</td>
<td>PCIe 8 GT/s Modified Compliance pattern for lane 0 for common reference as well as independent reference clock, version for error detector operating with SKP OS filtering</td>
</tr>
</tbody>
</table>

### PCI Express 4

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calibration/DMSI_CMSI_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/PCIe4_Compliance_lane0_BIT_16G</td>
<td></td>
</tr>
<tr>
<td>Calibration/RJ_SJ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/Step_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/TxEQ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Test/PCIe4_modified_compliance_lane_0_CC_BIT_16G</td>
<td>PCIe 16 GT/s Modified Compliance pattern for lane 0 for common reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/PCIe4_modified_compliance_lane_0_IR_BIT_16G</td>
<td>PCIe 16 GT/s Modified Compliance pattern for lane 0 for independent reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/PCIe4_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_16G</td>
<td>PCIe 16 GT/s Modified Compliance pattern for lane 0 for common reference as well as independent reference clock, version for error detector operating with SKP OS filtering</td>
</tr>
</tbody>
</table>
## PCI Express 5

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calibration/DMSI_CMSI_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/RJ_SJ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/Step_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/TxEQ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Test/PCIe5_modified_compliance_lane_0_CC_BIT_32G</td>
<td>PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for common reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/PCIe5_modified_compliance_lane_0_IR_BIT_32G</td>
<td>PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for independent reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/PCIe5_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_32G</td>
<td>PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for common reference as well as independent reference clock, version for error detector operating with SKP OS filtering</td>
</tr>
</tbody>
</table>

## PRBS

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRBS7_1-2_bit</td>
<td>PRBS 2^7 with a mark density of 1/2</td>
</tr>
<tr>
<td>PRBS7_1-8_bit</td>
<td>PRBS 2^7 with a mark density of 1/8</td>
</tr>
<tr>
<td>PRBS7_2-8_bit</td>
<td>PRBS 2^7 with a mark density of 2/8</td>
</tr>
<tr>
<td>PRBS7_6-8_bit</td>
<td>PRBS 2^7 with a mark density of 6/8</td>
</tr>
<tr>
<td>PRBS7_7-8_bit</td>
<td>PRBS 2^7 with a mark density of 7/8</td>
</tr>
<tr>
<td>PRBS10_1-2_bit</td>
<td>PRBS 2^10 with a mark density of 1/2</td>
</tr>
<tr>
<td>PRBS10_1-8_bit</td>
<td>PRBS 2^10 with a mark density of 1/8</td>
</tr>
<tr>
<td>PRBS10_2-8_bit</td>
<td>PRBS 2^10 with a mark density of 2/8</td>
</tr>
<tr>
<td>PRBS10_6-8_bit</td>
<td>PRBS 2^10 with a mark density of 6/8</td>
</tr>
<tr>
<td>PRBS10_7-8_bit</td>
<td>PRBS 2^10 with a mark density of 7/8</td>
</tr>
<tr>
<td>PRBS11_1-2_bit</td>
<td>PRBS 2^11 with a mark density of 1/2</td>
</tr>
<tr>
<td>Pattern</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>PRBS11_1-8_bit</td>
<td>PRBS 2^11 with a mark density of 1/8</td>
</tr>
<tr>
<td>PRBS11_2-8_bit</td>
<td>PRBS 2^11 with a mark density of 2/8</td>
</tr>
<tr>
<td>PRBS11_6-8_bit</td>
<td>PRBS 2^11 with a mark density of 6/8</td>
</tr>
<tr>
<td>PRBS11_7-8_bit</td>
<td>PRBS 2^11 with a mark density of 7/8</td>
</tr>
<tr>
<td>PRBS13_1-2_bit</td>
<td>PRBS 2^13 with a mark density of 1/2</td>
</tr>
<tr>
<td>PRBS13_1-8_bit</td>
<td>PRBS 2^13 with a mark density of 1/8</td>
</tr>
<tr>
<td>PRBS13_2-8_bit</td>
<td>PRBS 2^13 with a mark density of 2/8</td>
</tr>
<tr>
<td>PRBS13_6-8_bit</td>
<td>PRBS 2^13 with a mark density of 6/8</td>
</tr>
<tr>
<td>PRBS13_7-8_bit</td>
<td>PRBS 2^13 with a mark density of 7/8</td>
</tr>
<tr>
<td>PRBS15_1-2_bit</td>
<td>PRBS 2^15 with a mark density of 1/2</td>
</tr>
<tr>
<td>PRBS15_1-8_bit</td>
<td>PRBS 2^15 with a mark density of 1/8</td>
</tr>
<tr>
<td>PRBS15_2-8_bit</td>
<td>PRBS 2^15 with a mark density of 2/8</td>
</tr>
<tr>
<td>PRBS15_6-8_bit</td>
<td>PRBS 2^15 with a mark density of 6/8</td>
</tr>
<tr>
<td>PRBS15_7-8_bit</td>
<td>PRBS 2^15 with a mark density of 7/8</td>
</tr>
<tr>
<td>PRBS23_1-2_bit</td>
<td>PRBS 2^23 with a mark density of 1/2</td>
</tr>
<tr>
<td>PRBS23_1-8_bit</td>
<td>PRBS 2^23 with a mark density of 1/8</td>
</tr>
<tr>
<td>PRBS23_2-8_bit</td>
<td>PRBS 2^23 with a mark density of 2/8</td>
</tr>
<tr>
<td>PRBS23_6-8_bit</td>
<td>PRBS 2^23 with a mark density of 6/8</td>
</tr>
<tr>
<td>PRBS23_7-8_bit</td>
<td>PRBS 2^23 with a mark density of 7/8</td>
</tr>
<tr>
<td>PRBS7_1-2_bit</td>
<td>PRBS 2^7-1 with a mark density of 1/2</td>
</tr>
<tr>
<td>PRBS9_950_bit</td>
<td>PRBS 2^9-1 with the polynomial x^9+x^5+1</td>
</tr>
</tbody>
</table>
### SAS

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTPAT_b8b10</td>
<td>Jitter Tolerance Pattern (JTPAT) Minus</td>
</tr>
<tr>
<td>SAS_CJTPAT_Repeat_w_all_aligns_b8b10</td>
<td>CJTPAT framed for SAS; includes ALIGNs; uses B8B10 format</td>
</tr>
<tr>
<td>SAS_IDLE_CJTPAT_IDLE_ALIGNO_b8b10</td>
<td>IDLE, CJTPAT, IDLE framed for SAS; includes ALIGN 0; uses B8B10 format</td>
</tr>
<tr>
<td>scrambled_0-from-grex-demo-board_b8b10</td>
<td>Scrambled 0 pattern captured from G-Series scope demo board; uses B8B10 format</td>
</tr>
</tbody>
</table>

### SATA

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALIGN_b8b10</td>
<td>Align primitive as defined in SATA standard.</td>
</tr>
<tr>
<td>COMP-long-2.6spec_b8b10</td>
<td>Long COMP pattern starting with negative running disparity as defined in SATA standard version 2.6</td>
</tr>
<tr>
<td>COMP-long-framed_b8b10</td>
<td>Obsolete long framed COMP pattern</td>
</tr>
<tr>
<td>COMP-long_b8b10</td>
<td>Long COMP pattern starting with negative running disparity as defined in SATA standard version 2.5</td>
</tr>
<tr>
<td>COMP-short-2.6spec_b8b10</td>
<td>Short COMP pattern starting with negative running disparity as defined in SATA standard version 2.6</td>
</tr>
<tr>
<td>COMP-short_b8b10</td>
<td>Short COMP pattern as defined in SATA standard version 2.5</td>
</tr>
<tr>
<td>Framed_COMP_20070905_2ALIGNs_newLBP_92160_b8b10</td>
<td>Long framed COMP according to SATA standard version 2.6 with 2 ALIGNs</td>
</tr>
<tr>
<td>Framed_COMP_20070907_2ALIGNs_oldLBP_92160_b8b10</td>
<td>Long framed COMP according to SATA standard version 2.5 with 2 ALIGNs</td>
</tr>
<tr>
<td>HFTP_b8b10</td>
<td>SATA High Frequency Test Pattern</td>
</tr>
<tr>
<td>HFTP_w_align_b8b10</td>
<td>SATA High Frequency Test Pattern; includes ALIGNs; uses B8B10 format</td>
</tr>
<tr>
<td>HTDP_long_b8b10</td>
<td>SATA long high transition density pattern</td>
</tr>
<tr>
<td>HTDP_short_b8b10</td>
<td>SATA long high transition density pattern</td>
</tr>
<tr>
<td>LBPspecv2.5-short-w-align_b8b10</td>
<td>SATA lone bit pattern according to SATA standard version 2.5; includes ALIGNs; uses B8B10 format</td>
</tr>
<tr>
<td>LBP_long-2.6spec_b8b10</td>
<td>SATA short lone bit pattern according to SATA standard version 2.6</td>
</tr>
<tr>
<td>LBP_long_b8b10</td>
<td>SATA long lone bit pattern according to SATA standard version 2.5</td>
</tr>
</tbody>
</table>
## USB 3.0

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock_bit</td>
<td>clk/2 pattern; uses BIT format</td>
</tr>
<tr>
<td>D0_SCRAMMBLED_b8b10</td>
<td>scrambled D0; uses B8B10 format</td>
</tr>
<tr>
<td>K25_K27_2SKP_b8b10</td>
<td>debug pattern; uses B8B10 format</td>
</tr>
<tr>
<td>K285_D0_b8b10</td>
<td>debug pattern; uses B8B10 format</td>
</tr>
<tr>
<td>LFPS_BURST_1us_IDLE_9us_bit</td>
<td>part of trainings sequence; uses BIT format</td>
</tr>
<tr>
<td>LFPS_IDLE_9us_BURST_1us_bit</td>
<td>part of trainings sequence; uses BIT format</td>
</tr>
<tr>
<td>LFPS_TRIGGER_bit</td>
<td>part of trainings sequence; uses BIT format</td>
</tr>
<tr>
<td>TS1_31_2SKP_b8b10</td>
<td>part of trainings sequence; uses B8B10 format</td>
</tr>
<tr>
<td>TS1_31_4SKP_b8b10</td>
<td>part of trainings sequence; uses B8B10 format</td>
</tr>
<tr>
<td>TS2_2SKP_b8b10</td>
<td>part of trainings sequence; uses B8B10 format</td>
</tr>
<tr>
<td>TS2_4SKP_b8b10</td>
<td>part of trainings sequence; uses B8B10 format</td>
</tr>
<tr>
<td>TSEQ_b8b10</td>
<td>part of trainings sequence; uses B8B10 format</td>
</tr>
<tr>
<td>BRST_2SKP_b8b10</td>
<td>part of trainings sequence; uses B8B10 format</td>
</tr>
</tbody>
</table>

### SATA Patterns

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LBP_short-2.6spec_b8b10</td>
<td>SATA long lone bit pattern according to SATA standard version 2.6</td>
</tr>
<tr>
<td>LBP_short_b8b10</td>
<td>SATA short lone bit pattern according to SATA standard version 2.5</td>
</tr>
<tr>
<td>LFSCP_long_b8b10</td>
<td>SATA long low frequency spectral content pattern</td>
</tr>
<tr>
<td>LFSCP_short_b8b10</td>
<td>SATA short low frequency spectral content pattern</td>
</tr>
<tr>
<td>LTDP_long_b8b10</td>
<td>SATA long low transition density pattern</td>
</tr>
<tr>
<td>LTDP_short_b8b10</td>
<td>SATA short low transition density pattern</td>
</tr>
<tr>
<td>MFTP_b8b10</td>
<td>SATA mid frequency test pattern</td>
</tr>
<tr>
<td>SSOP_long_b8b10</td>
<td>SATA short simultaneous switching outputs pattern starting</td>
</tr>
<tr>
<td>SSOP_short_b8b10</td>
<td>SATA short simultaneous switching outputs pattern starting</td>
</tr>
<tr>
<td>k28.5_b8b10</td>
<td>K28.5 symbols; uses B8B10 format</td>
</tr>
</tbody>
</table>
### BRST_4SKP_b8b10
- Part of trainings sequence; uses B8B10 format

### COMMA_2SKP_b8b10
- Debug pattern; uses B8B10 format

### COMMA_4SKP_b8b10
- Debug pattern; uses B8B10 format

### CP0_2SKP_SCRAMbled_b8b10
- CP0 compliance pattern containing SKP doubles; pre-scrambled; uses B8B10 format

### CP0_2SKP_for_SER_b8b10
- CP0 compliance pattern containing SKP doubles; pre-scrambled; uses B8B10 format

### CP0_4SKP_for_SER_b8b10
- CP0 compliance pattern containing SKP doubles; pre-scrambled; uses B8B10 format

### Clock16_bit
- clk/16; uses BIT format

### Clock8_bit
- clk/8; uses BIT format

### Clock4_bit
- clk/4; uses BIT format

### Clock2_bit
- clk/2; uses BIT format

### UniPro1-LaneCJTPAT_b8b10
- Pattern used for M-PHY Rx jitter tolerance test for 1 lane UniPro (CJTPAT, 8b/10b encoded).

### UniPro1-LaneCJTPAT_bit
- Pattern used for M-PHY Rx jitter tolerance test for 1 lane UniPro (CJTPAT, bit pattern).

### UniPro1-LaneCRPAT_b8b10
- Pattern used for M-PHY Tx test for 1 lane UniPro (CRPAT, 8b/10b encoded).

### UniPro1-LaneCRPAT_bit
- Pattern used for M-PHY Tx test for 1 lane UniPro (CRPAT, bit pattern).

### UniPro2-LaneCJTPAT-Lane0_b8b10
- Pattern used for M-PHY Rx jitter tolerance test for lane 1 of 2 UniPro (CJTPAT, 8b/10b encoded).
### IEEE

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP03A_bit</td>
<td>IEEE802.3bj clause 94.2.9.1 for 100GBASE-KP4. The JP03A test pattern is generated prior to PAM4 encoding. JP03A pattern is a repeating (0,3) sequence.</td>
</tr>
<tr>
<td>JP03B_bit</td>
<td>IEEE802.3bj clause 84.2.9.2 for 100GBASE-KP4. The JP03B test pattern is generated prior to PAM4 encoding. The JP03B pattern is a repeating sequence of (0,3) repeated 15 times followed by (3,0) repeated 16 times.</td>
</tr>
<tr>
<td>PAM4_Linearity_Test_bit</td>
<td>IEEE 802.3bj clause 94.2.9.4 transmitter linearity test pattern. To get correct output symbols the respective generator needs to have Uncoded selected.</td>
</tr>
<tr>
<td>PRBS13Q_Lane0_bit</td>
<td>PRBS13Q Lane 0 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
<tr>
<td>PRBS13Q_Lane1_bit</td>
<td>PRBS13Q Lane 1 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
<tr>
<td>PRBS13Q_Lane2_bit</td>
<td>PRBS13Q Lane 2 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
<tr>
<td>PRBS13Q_Lane3_bit</td>
<td>PRBS13Q Lane 3 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
<tr>
<td>QPRBS13_Lane0_bit SelectGrayCoded</td>
<td>QPRBS13 Lane 0 pattern as defined in IEEE 802.3 clause 94.2.9.3. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
<tr>
<td>SSPRQ_bit SelectGrayCoded</td>
<td>SSPRQ pattern as defined in IEEE 802.3 clause 120.5.11.2.5. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
<tr>
<td>SSPRQ_bit SelectGrayCoded_D1p5</td>
<td>SSPRQ pattern as defined in IEEE 802.3 clause 120.5.11.2.5. To get correct output symbols the respective generator needs to have Gray Coding selected.</td>
</tr>
</tbody>
</table>
### USB3.0_LTSSM

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRST_Bit</td>
<td>BRST</td>
</tr>
<tr>
<td>loopbackED_B8B10</td>
<td>CP0 for ED</td>
</tr>
<tr>
<td>loopbackPG_Bit</td>
<td>CP0 for PG</td>
</tr>
</tbody>
</table>

### USB3.1_LTSSM

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP9_BLOCK_ANALYZER_B128B132</td>
<td>CP9 for ED</td>
</tr>
<tr>
<td>CP9_BLOCK_GENERATOR_B128B132</td>
<td>CP9 for PG</td>
</tr>
<tr>
<td>IDLE_B128B132</td>
<td></td>
</tr>
</tbody>
</table>

### CCIX

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calibration/DMSI_CMSI_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/RJ_SJ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/Step_BIT</td>
<td></td>
</tr>
<tr>
<td>Calibration/TxEQ_cal_BIT</td>
<td></td>
</tr>
<tr>
<td>Test/CCIX_modified_compliance_lane_0_CC_BIT_20G_25G</td>
<td>CCIX Modified Compliance pattern for lane 0 for common reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/CCIX_modified_compliance_lane_0_IR_BIT_20G_25G</td>
<td>CCIX Modified Compliance pattern for lane 0 for independent reference clock, version for pattern generator</td>
</tr>
<tr>
<td>Test/CCIX_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_20G_25G</td>
<td>CCIX Modified Compliance pattern for lane 0 for common reference as well as independent reference clock, version for error detector operating with SKP OS filtering</td>
</tr>
</tbody>
</table>
### PAM3

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRBS11-1_PAM3_2-bits-per-symbol_bit</td>
<td>PRBS11-1 pattern to be used if PAM3 encoding is selected. It is two bits per symbol and only values 0 and 2 are occurring.</td>
</tr>
<tr>
<td>PRTS7-1_PAM3_2-bits-per-symbol_bit</td>
<td>PRTS7-1 pattern to be used if PAM3 encoding is selected. Two bits per symbol and values 0, 1 and 2 may occur. Polynomial: 1+2x^2+x^7</td>
</tr>
<tr>
<td>PRTS7-1_precoded_PAM3_2-bits-per-symbol_bit</td>
<td>Like PRTS7-1 above but data is encoded with Data_Out=modulo3(Data_In + Sequence)</td>
</tr>
</tbody>
</table>

### FEC

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlignmentMarkers_802_3cd</td>
<td>IEEE802.3 MAC control word (0x1E) which is Reed Solomon Encoded and formatted according to IEEE802.3cd</td>
</tr>
<tr>
<td>IEEE_802_3cd_RS_544_514_Remote_Fault</td>
<td>IEEE802.3 MAC control word (0x00) which is Reed Solomon Encoded and formatted according to IEEE802.3cd</td>
</tr>
<tr>
<td>IEEE_802_3cd_RS_544_514_Scrambled_Idle</td>
<td>IEEE802.3 MAC control word (0x00) which is Reed Solomon Encoded and formatted according to IEEE802.3cd</td>
</tr>
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