PCI Express® Revision 2 Receiver (RX) Jitter Tolerance Test

with J-BERT N4903B
High-Performance Serial BERT

Application Note

J-BERT N4903B
High-Performance Serial BERT with Complete Jitter Tolerance Testing for PCI Express® Revision 2

• All jitter sources built in (dual tone DJ, spectral RJ, SSC and residual SSC) compliant to PCI Express® revision 2
• Flexible clock and trigger channels to support PCI Reference clock differential mode noise
• Flexible pattern sequencer to train the DUT (set loop-back mode) and run the test
• J-BERT N4903B high performance serial BERT’s automated compliance tests with N5990A test automation software
Scope of this document

This document describes the RX jitter tolerance test requirements for PCI Express revision 2. It explains how these requirements can be efficiently fulfilled for compliance and characterization test with help of the J-BERT N4903B high-performance serial BERT with complete jitter tolerance testing.

Finally there is a short introduction on TX testing with help of the measurements of the J-BERT N4903B.

Introduction

PCI Express made it to one of the major interfaces inside a computer. In December 2006 the PCI-SIG® association released the base specification revision 2 [1]. The revision 2 doubles the operating speed from 2.5 Gb/s in revision 1 to 5 Gb/s. Beside the base specification there was a release of the card electromechanical (CEM) specification, revision 2.0 in April 2007 [2] as a companion to the base specification.

From testing perspective the two specifications can be treated as: the base specification deals with performance at chip level, while the CEM specification deals with the cards at the connectors especially in the case of interoperability.

Requirements by the standards

The base specification deals with two different clocking topologies called:
- Data driven topology
- Common reference clock

Simply said the first does not share a clock signal, while the second provides a common reference clock at 1/50 of the data rate. The first two columns in Table 1 represent the two test cases and the according jitter parameter values.

The CEM standard deals with add-in card and system board test for the common reference clock topology. The last two columns in Table 1 represent the jitter parameter values for these two test cases. Consecutively Table 1 lists the jitter parameters for the four RX test cases. In the following these parameters are described in more detail:

1. The calibration channel applies in the base specification. It intends to create inter-symbol interference (ISI) described as an amplitude ratio of 5:1. The intention is to create a signal aberration which is apparent in printed circuit boards used for the motherboard and the add-in card. A signal with this amplitude ratio can be obtained from ISI trace 3 in J-BERT N4903B as shown in Figure 1. The marker read-outs provide the desired ratio. This incorporates a timing jitter of 73 ps (ISI reading) as can be seen on Figure 2. With the specification of DJ (1.5 MHz .. 100 MHz) with value of 88 ps, there is a remaining need for SJ by 15 ps.

2. All the following jitter parameters are calibrated dials on the J-BERT N4903B. There is no need for any calibration. Just enter the desired values in the dials as shown in Figure. If it is intended to verify the jitter values, the use of the infinium 86100C DCA-J is recommended with help of the jitter analysis as shown in Figure 2 (RJ, PJ & ISI readings) in accordance with the application note [7].

<table>
<thead>
<tr>
<th>PCIe 2nd RX test</th>
<th>Chip test</th>
<th>Chip test</th>
<th>Add-in test</th>
<th>System board</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Base spec</td>
<td>Base spec</td>
<td>CEM spec</td>
<td>CEM spec</td>
</tr>
<tr>
<td>Calibration</td>
<td>channel (ISI)</td>
<td>5 : 1 pulse voltage</td>
<td>5 : 1 pulse voltage</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>RJ 1.5 MHz .. 100 MHz</td>
<td>4.2 ps rms</td>
<td>3.4 ps rms</td>
<td>3.4 ps rms</td>
</tr>
<tr>
<td></td>
<td>RJ 10 kHz .. 1.5 MHz</td>
<td>8.0 ps rms</td>
<td>4.2 ps rms</td>
<td>4.2 ps rms</td>
</tr>
<tr>
<td></td>
<td>DJ &gt; 100 MHz</td>
<td>No</td>
<td>No</td>
<td>Yes, SJ of 27 ps</td>
</tr>
<tr>
<td></td>
<td>DJ &gt; 1.5 MHz .. 100 MHz</td>
<td>Yes, pure SJ or (SJ + ISI) of 88 ps</td>
<td>Yes, SJ of 30 ps</td>
<td>Yes, SJ of 30 ps</td>
</tr>
<tr>
<td></td>
<td>Desidual SSC</td>
<td>No</td>
<td>75 ps, triangle</td>
<td>75 ps, triangle</td>
</tr>
<tr>
<td></td>
<td>SSC</td>
<td>20 ns (-500 ppm)</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>CM crosstalk (SI)</td>
<td>300 mV</td>
<td>300 mV</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>VRX-eye, min</td>
<td>100 mV pp, diff</td>
<td>120 mV pp, diff</td>
<td>300 mV pp, diff</td>
</tr>
</tbody>
</table>

Table 1: Parameters for RX Jitter Tolerance Testing required for the different test cases
3. RJ (1.5 MHz .. 100 MHz) applies in all test cases with various amount.

4. RJ (10 kHz .. 1.5 MHz) applies in all test cases with various amount.

5. DJ > 100 MHz applies in the CEM standard as a replacement of the ISI generation in the base specification.

6. DJ (1.5 MHz .. 100 MHz) applies in all test cases with various amount. With help of the jitter tolerance measurement it is possible to sweep the frequency for debug/characterization testing.

7. Residual SSC applies to both standards but not for system board test. This is similar to a periodic jitter but with a triangular shape.

8. SSC applies in the base specification for the data driven topology only. SSC is again a calibrated dial located in the N4903B generator clock setup window. SSC is the only jitter component which can’t be measured directly with the jitter analysis on the infiniium 86100C DCA-J; instead a spectrum analyzer is recommended, more details are given in [6].

9. The bottom row values in Table 1 refer to the required minimum amplitudes. The amplitudes are intended at the chip pin. Due to the loss of the PC board, these amplitude are different from the amplitudes at the end of the coaxial cables. Furthermore the Gen2 standard requires the loss compensation the way that the transitional bit and the de-emphasized bit have the same amplitude. This makes it necessary to use the N4916A de-emphasis signal converter as shown in Figure 3. For add-in card test according the CEM spec the calibration of the minimum amplitude can be performed with help of the compliance base board (CBB) and the compliance load board (CLB), both provided by the PCI SIG, where the coaxial cables hook up conveniently. The N4916A signal converter is used to dial in its variable de-emphasis until the amplitudes of the transitional bit and the amplitude of the de-emphasized bit are the same. [8]
More PCI Express revision 2 RX test jitter fundamentals

PCI Express Revision 2 RX Jitter tolerance testing deals with new kind of jitter creation for stressing the RX:

1. Spectrally distributed RJ
2. Dual tone DJ
3. Residual SSC

This chapter is intended to look a little deeper into these subjects:

Figure 4 shows spectrally distributed RJ. The diagram shows the amount of jitter vs. frequency. White noise (unlimited bandwidth) contains constant amount of energy at all frequencies. The specification here intends a higher amount of random jitter at the lower frequencies and a lower amount at the higher frequencies. The actual amount depends on the test case, see Table 1. The corner frequency is at 1.5 MHz, the filter cut-off shall be infinitely steep (Brick-wall filter).

J-BERT N4903B creates this scenario by RJ$_{lf}$ over the whole bandwidth (10 kHz .. 100 MHz) and adds RJ$_{hf}$ (10 kHz .. 1.5 MHz) on top.

Figure 5 shows the concept of dual tone DJ. Normally DJ jitter would be used as sinusoidal jitter at one frequency while the frequency may be varied over time (jitter tolerance measurement). The dual tone method uses two sinusoidal signals at the same time, one at the lower and one at higher frequency.

Optionally the signal at lower frequency may sweep continuously between the min. and max. value of the frequency band. The actual amount of both signals depend on test case, see Table 1. J-BERT N4903B creates PJ1 and PJ2 accordingly.

Figure 6 shows the spread-spectrum modulation (SSC). Such a modulation is defined by the SSC deviation (typ. 500 ppm) and the SSC frequency (typ. 30 .. 33 kHz). The deviation occurs downwards typically. So for a data rate of 5 Gb/s the deviation of 500 ppm means the data rate changes between 5 Gb/s and 4.975 Gb/s with a frequency of 30 .. 33 kHz. The shape of the ideal modulation is triangular, while practically anything between sinusoidal and triangular is applied.
Figure 7 depicts the SSC modulation in time view. The top trace is a signal without SSC for reference. With the bottom trace the data signal is shown while the SSC modulation starts with the negative slope. On this slope the data rate (in frequency) decreases linear; the data cycle (in time) increases by the function \(1/x\). With a SSC frequency of 33 kHz the duration of the negative slope lasts 15 us. So there are:

\[
15 \text{ us}/200\text{ps} = 75000 \text{ data cycles (1)}
\]

along the negative transition. The change in time for the data cycle is from 200 ps (\(D_1\)) to 201,005 ps (\(D_{75000}\)). The total delay shift of the data stream in reference to the unmodulated signal is as much as \(T_{\text{SSC}} = 20\text{ ns}\) from the beginning to the end of the negative transition of the modulation:

\[
T_{\text{SSC}} = \sum (D_n - 200\text{ps}), n = 1 .. 75000 \quad (2)
\]

PCIe adds the SSC modulation to the 100 MHz refclk, consequently the system needs a multiplying PLL in the TX and a multiplying PLL with clock-data recovery (CDR) in the RX. A CDR has a finite bandwidth, causing a finite time for reacting on the refclk changes. A system architecture as shown in Figure 8, incorporates a significant difference in transport delay for the TX data appearing at the RX latch input and the clock running through the CDR. The transport delay through the CDR (~ 200 ns) is much higher than through the channel (spec is < 12 ns). Such delay difference results in phase shift of the SSC causing eye closure at the sampler. This is called, residual SSC (rSSC). When testing this matter is inverted by using a clean refclk and residual SSC on the data which creates an equivalent stress situation.

Figure 6: SSC modulation

Figure 7: SSC modulation in time view

Figure 8: Transport delay differences cause residual SSC (rSSC)
Test setup, block architecture

Figure 9 to 11 illustrate the RX test setups as block diagrams.

The base specification applies to the device under test (DUT) on a chip level. Custom designed boards to accommodate the chips are necessary. These designs may or may not include the calibration channel. If not, the ISI capability of J-BERT N4903B may be used.

Depending on the clock topology the J-BERT N4903B connects to the board with generator data and error detector and with or without reference clock. For the reference clock it is recommended to use the trigger channel, see next page and Figure 12.

The CEM specification applies to the add-in card test (Figure 10) and system board test (Figure 11). For these tests the compliance base board (CBB) and the compliance load board are necessary [3], [4]. It may be necessary to apply modification to the CBB for proper reference clock injection, see [5].

For the test of an add-in card with more than one data lane a PCIe-Riser-Card x1 to 1x PCIe x16 is recommended.

Testing according CEM specification is in general according the reference clock topology. So the J-BERT N4903B connects with generator data, error detector and the trigger channel as reference clock, see above.
Test Setup, J-BERT N4903B Settings

J-BERT N4903B connects with generator data out, error detector data in and the trigger channel as a reference clock if needed. The trigger channel can be programmed in amplitude and offset to apply the required level specifications as shown in Figure 12. The trigger channel is able to supply a clock signal with a divider factor of 1/50 to supply the reference clock at 100 MHz (this programming window is not shown, it is accessible with the button PG Setup → Trigger/Ref CIC Setup).

Figure 13 shows the J-BERT N4903B sequence editor with the sequence necessary to train the add-in card. The training consists of the top three blocks, which bring the add-in card into the loop-back mode. Block 4 contains the compliance pattern, which will be used on the error detector for synchronization and BER measurement. The sequence is loaded into the J-BERT N4903B hardware by pressing the button, To PG`. Before pressing the ‘Start’ button, the add-in card should be powered. When pressing the ‘Start’ button the sequence is generated by sending block 1 & 2 once, block 3 times 500 and finally block 4 for infinite. This is indicated in the left bottom status window reading ‘Sequence, B:4’. At this point the J-BERT error detector can be auto-aligned resulting in the ‘BER:0.000’ reading. Not shown is that the J-BERT N4903B error detector gets the clock from the generator clock output in ext. clock mode. (ED Setup → Clock Setup).

Figure 14 shows the jitter setup for the add-in card test scenario. The values dialed in:

- rSSC (spec is 75 ps)  375 mUI
- PJ1(<100 MHz, 30 ps)  150 mUI
- PJ2 (> 100 MHz, 27 ps)  135 mUI
- sRJ (HF, 3.4 ps rms)  17 mUI rms
- sRJ (LF, 4.2 ps rms)  4 mUI rms

Note: The implementation of RJLF is incremental; the programming value calculates: RJLF-RJHF = 4.2 ps rms - 3.4 ps rms = 0.8 ps rms (equals 4 mUI rms)

With this mix of jitter components the add-in card has to work for a BER < 1e-12 to be standard compliant.
RX Test Results

The verification of the compliance of an add-in card can be effectively performed with help of the ‘accumulated results’, as shown in Figure 15. To prove the BER $< 1 \times 10^{-12}$ with a confidence level of 95% it is necessary to test $\sim 3 \times 10^{12}$ bits without an error [9]. This equals 600 sec test time at the data rate of 5 Gb/s. The accumulated result measurement is configured for single run and 600 sec duration. The resulting graph will tell if any error occurred.

For characterization or debug testing the jitter tolerance characterization measurement is a meaningful tool, as shown in Figure 16. The measurement can be configured for start and end of tolerance sweep and resolution and can be zoomed as desired. Optional a compliance mask can be loaded to see the margin. The faster version is the jitter tolerance compliance measurement, where the measured point are along the compliance curve. Figure 16 runs the tolerance measurement from 1 kHz to 300 MHz with 50 points.

While the specifications state the RX compliance testing is performed with non-de-emphasized signals, for characterization purpose it may be desirable to use such signals. In this case it is recommended to use the N4916A de-emphasis signal converter, for details see [8].

TX Test Results

TX compliance test is efficiently performed with help of the J-BERT N4903B eye diagram measurement and the ability to load a predefined compliance mask with margin definition, as shown in Figure 17. This measurement is fast and quantifies any violations (yellow insert). Beside the fit to the compliance mask the measurement provides the readings for levels, amplitude, transition time, jitter and signal-to-noise ratio.
The J-BERT N4903B provides various measurements for characterization of the TX. Figure 18 & 19 show as examples the eye opening and the output timing measurement. The J-BERT N4903B data sheet (5990-3217EN) provides the full list of measurement capabilities.

The eye diagram in Figure 18 provides the eye contour measurement of the output signal of an add-in card down to BER 1 e-9 (red curve) with a resolution of 1 mV in amplitude and 1 ps in time.

The output timing measurement in Figure 19 is able to measure the total jitter at mostly any BER threshold, the graph shown here is configured for BER 1e-6. With the fast total jitter optimization enabled, the measurement on the total jitter for BER < 1e-12 will be completed in roughly 20 min.

Figure 20 shows a measurement of the TX Jitter Transfer. This measurement is done by manual sweep of the jitter frequency (SJ = .1 UI, 500 kHz .. 50 MHz) and record of the phase margin parameter of output timing measurement. The values are entered into a spreadsheet and normalized to the reading at lowest jitter frequency. Figure 20 represents the resulting graph for the TX jitter transfer.

**Summary**

This document describes the requirements for PCI Express revision 2 RX jitter tolerance intended by the base and CEM standards. These standards set some new kind of jitter creation requirements, which are discussed in depth. The document highlights the capabilities of the J-BERT N4903B to efficiently address these new requirements. Finally there is some outlook provided to address TX test need with the J-BERT N4903B.

The J-BERT N4903B provides all jitters as calibrated dials, so without any need for a custom calibration. In case of de-emphasized signals are desired, the use of N4916A de-emphasis signal converter is recommended.
Remove all doubt

Our repair and calibration services will get your equipment back to you, performing like new, when promised. You will get full value out of your Agilent equipment throughout its lifetime. Your equipment will be serviced by Agilent-trained technicians using the latest factory calibration procedures, automated repair diagnostics and genuine parts. You will always have the utmost confidence in your measurements.

For more information regarding self maintenance of this product, please contact your Agilent office.

Agilent offers a wide range of additional expert test and measurement services for your equipment, including initial start-up assistance, onsite education and training, as well as design, system integration, and project management.

For more information on repair and calibration services, go to:

www.agilent.com/find/removealldoubt

Product specifications and descriptions in this document subject to change without notice.

PCI-SIG and the PCI SIG design marks are registered trademarks and/or service marks of PCI-SIG.

Agilent Email Updates

www.agilent.com/find/emailupdates

Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect

Quickly choose and use your test equipment solutions with confidence.