Presentation on Trends in Signal Integrity Tests

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Trends in Signal Integrity Test

Parametric Test for High-Speed Serial Technologies

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High Speed Digital Test
Agenda

• Trend and Challenges Testing High-Speed Serial Technologies
  • Trends in High-Speed Serial Markets
  • New Challenges for Designers
  • Physical Layer Test Challenges

• Receiver Tolerance Testing
  • What do Standards require
  • The Importance of the Receiver
  • How to implement Jitter Emulation

• Agilent’s Strategy to Address the New Requirements
High Speed Market Segments & Technologies

### Computing
- Processor Bus
- Memory Bus
- Peripheral Bus

### Enterprise
- SAN
- LAN

### Public Network
- Communications Bus
- Access
- Metro
- Long Haul

#### Hot markets
- SONET OC-3
- SONET OC-12
- G-PON
- E-PON
- SONET OC-48
- SONET OC-192
- SONET OC-768

#### Speed (Gb/s)
- 40.0
- 10.0
- 1.0
- 0.1

#### Technologies
- FBD-I
- FBD-II
- SATA III
- PCI Express-I/II
- SATA II
- RapidIO
- 10x FC
- 8x FC
- 4x FC
- 2x FC
- 1G Ethernet
- 10G Ethernet
- CEI 6G
- CEI 11G
Serial busses are becoming mainstream

As data rates go to 3, 5, and 6 Gb/s and beyond, technical challenges are increasing disproportionately.

- PCI Express at 2.5 going to 5 Gb/s
- SATA/SAS at 1.5, moves to 3 and 6 Gb/s
- FBD at 4.8 going to 9.8 Gb/s
- CEI defining tests for 6 and 11 Gb/s
- External communications for computers:
  - Various Ethernet standards to 10 Gb/s
  - Fibre Channel to 10 Gb/s
Physical layer testing trends

Many players/vendors: *Tests and specs designed to maximize interoperability*

Volume production: *Avoid high-speed test by minimizing sensitivity to manufacturing variations*

- Heavy burden on R&D to get it right
- Expertise on the entire system (TX/Channel/RX)
- Design change in one area must be validated versus others
- Typical digital engineer toolbox running out of steam
- Required Jitter tests are time consuming and complex
The new communications system

A bus is now to be viewed as a communications system even though spans are measured in inches or centimeters
Low-cost channels become lossy and dispersive

A Channel requires accurate characterization for impedance and transmission characteristics including equalization and interactions with TX and RX

TDR and VNA characterize the channel alone
Transmitters must compensate for low-cost cables and boards

Pre-emphasized signal analysis (optimized signal versus channel performance), precision waveform characterization for compliance

Tools available today for complete solution
Receivers must tolerate degraded signals

Precisely “impaired data streams” are required to verify receiver robustness. Calibrated composition of various types of jitter (RJ, PJ, BUJ, ISI, SI) is required to generate real-world stress.

BERTs are offering complete Jitter Tolerance Test capabilities in one box. Opportunity to reduce complexity and automate testing.
Systems must tolerate low-cost clock sources

Phase noise analysis complements jitter analysis for clock characterization

Currently a very difficult measurement. Opportunity for PLL characterization techniques using phase noise approach
Emerging test requirements

What is needed:

• Ability to easily analyze all aspects of the Tx/Ch/Rx/RefClk and treat them as a complete communications system, rather than individual components.

• Efficiency – provide the right toolset to get to fast and accurate test results despite the overall complexity of Signal Integrity and the Jitter topic.

• Ease of use - let engineers focus on analyzing their designs rather than learning how to use test equipment.

• Confidence in measurement results - repeatability from one test system to the next.

• Accurate, complete & affordable measurement capabilities.
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The most neglected topic: the RX input

Where to use the BERT?

**TX Test:**
- Stimulate with any Pattern Generator or built-in BIST
- Measure with Scope (real-time, sampler), BERT Analyzer

**RX Test:**
- Stimulate with BERT Generator (any generator with jitter capabilities)
- Analyze with BERT Analyzer
RX Specification

1st: Compliance Eye
2nd: Jitter Tolerance Curve
3rd: Dynamic Voltage Range

\[ V_{RX\_MIN\_MAX\_RATIO} = \frac{V_{SWING\_MAX}}{V_{SWING\_MIN}} \]
Figure 7-9: Required receiver input eye (differential) showing minimum voltage and timing specs.
RX Spec: Jitter Tolerance Mask

In-band jitter
PLL/CDR follows
-> no big issue

Out-band jitter
Beyond PLL/CDR bandwidth, causes eye closure
-> CRITICAL

Limited UI at low freq

Cut-off at fdata / 1667

Figure 47-5—Single-tone sinusoidal jitter mask
RX Spec: Dynamic Voltage Range

\[ V_{RX\_MIN\_MAX\_RATIO} = \frac{V_{SWING\_MAX}}{V_{SWING\_MIN}} \]

- Min. Pulse Width
- Min. Pulse Amplitude
- Amplitude Ratio

Differential zero crossing

2 UI

\[ V_{SWING\_MIN} \]

\[ V_{SWING\_MAX} \]

\[ TRX\_MIN\_PULSE \]
## Requirements by Standards

<table>
<thead>
<tr>
<th>Standards</th>
<th>Compliance Eye</th>
<th>Min. Pulse Width</th>
<th>Tolerance Curve</th>
<th>SJ/PJ</th>
<th>RJ</th>
<th>BUJ</th>
<th>ISI</th>
<th>SI (Stressed Eye)</th>
<th>SSC</th>
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<tr>
<td>PCIe 1.1</td>
<td>.4 UI</td>
<td>.4 UI</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>PCIe 2.0</td>
<td>.4 UI</td>
<td>.6 UI</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>10GbE</td>
<td>.7 UI</td>
<td>5 UI @ 40kHz</td>
<td>.1 UI</td>
<td>&lt;.25 UI</td>
<td>.1 UI</td>
<td>.1 UI</td>
<td>.1 UI</td>
<td>30kHz, 0/-5%</td>
<td></td>
</tr>
<tr>
<td>XAUI</td>
<td>.35 UI</td>
<td>8.5 UI @ 22kHz</td>
<td>.37 UI</td>
<td>.18 UI</td>
<td>.18 UI</td>
<td>.18 UI</td>
<td>.1 UI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CEI 6G / 11G</td>
<td>.35 UI</td>
<td>17 UI @ 2kHz</td>
<td>.15 UI</td>
<td>.2 UI</td>
<td>.25 UI</td>
<td>.25 UI</td>
<td>.25 UI</td>
<td>.05 UI</td>
<td></td>
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<tr>
<td>Fibre Channel 4.25 Gb/s</td>
<td>.38</td>
<td>1.5 UI @ 42.5 kHz</td>
<td>.33 UI</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td>.1 UI</td>
<td></td>
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<tr>
<td>FB-DIMM AMB 1.0/2.0</td>
<td>.4 UI</td>
<td>.55 UI</td>
<td>.5 UI @ 20kHz</td>
<td>.3 UI</td>
<td>.1 UI</td>
<td>.28 UI</td>
<td>.28 UI</td>
<td>30kHz, 0/-5%</td>
<td></td>
</tr>
<tr>
<td>XFI/XFP</td>
<td>.35</td>
<td>15 UI @ 2 kHz</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td>.2 UI</td>
<td></td>
</tr>
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<td>SATA II</td>
<td>.35 UI</td>
<td></td>
<td>.35 UI</td>
<td>.3 UI</td>
<td></td>
<td></td>
<td></td>
<td>30kHz, 0/-5%</td>
<td></td>
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</tbody>
</table>
PCle Gen2: Jitter Modulation Details
Jitter Tolerance Test Setup

- DCA-J (86100C)
- Serial BERT (N4901B)
- PSG Synthesizer (E8257C)
- Noise Generator (PNG7110)
- Pattern Generator (81133A)
- Fill Panel
- Fill Panel
- Fill Panel
- Fill Panel

With N4903A J-BERT

Accurate Jitter Injection capabilities built-in & calibrated
jHardware Overview

Integrated & calibrated Jitter Injection

Ext. Clock

Int. Clock

SJ/SSC

Triangle Sine PJ BUJ Ext In RJ +

Common / Differential Mode Noise

Sine

Clock Modulation

Delay Line

Sub-Rate Clock

Data

Trigger

ISI/SI +

Clock

Agilent Technologies
Sinusoidal (SJ) & Periodic (PJ) Jitter

Ideal clock: \[ \sin(2\pi f_c t) \]

Jittered clock: \[ \sin\left(2\pi f_c t + \frac{4}{5}\pi \sin\left(\frac{1}{10} 2\pi f_c t\right)\right) \]

Jitter: \[ \frac{1}{3} \pi \sin\left(\frac{1}{10} 2\pi f_c t\right) \]
Random Jitter: the Gaussian Distribution

General:
# events = n x σ (sigma)

Random Jitter: n(BER) x σ

<table>
<thead>
<tr>
<th>n</th>
<th># events</th>
<th>BER</th>
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<tr>
<td>2</td>
<td>67%</td>
<td>0.33</td>
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<tr>
<td>4</td>
<td>97%</td>
<td>0.03</td>
</tr>
<tr>
<td>6</td>
<td>99.7%</td>
<td>0.003</td>
</tr>
<tr>
<td>9.8</td>
<td>10⁶</td>
<td>10⁻⁶</td>
</tr>
<tr>
<td>12.2</td>
<td>10⁹</td>
<td>10⁻⁹</td>
</tr>
<tr>
<td>14.1</td>
<td>10¹²</td>
<td>10⁻¹²</td>
</tr>
</tbody>
</table>
BUJ: the bounded Distribution

- BUJ is sometimes also called ‘bounded RJ’
- Depending on PRBS polynomial, filter frequency and PRBS generation rate, other Jitter Histograms can be created (overlaying events, sometimes mathematically hard to describe)
Duty Cycle Distortion (DCD)

Single ended Signals

Differential Signal

Offset causes DCD
Inter-Symbol Interference (ISI)

1: 1-> 0 transition
2: 0 -> 1 transition
3: 1 UI pulse
Common and Differential Mode Noise

![Diagram showing common and differential mode noise](Image)

Differential Signals:
- Edge Modulation
- Level Modulation

Common Mode Noise

Differential Mode Noise
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DSO 80000 Infiniium Oscilloscope

13 GHz Real-time Oscilloscope:
- EZJIT Plus Jitter Analysis Software
- 1160 Series InfiniiMax Active Differential Probes
- 40 GSa/s, 4 Channels
- Compliance Test Software packages for PCI Express, FBD, DDR2, SATA, SAS, FC, Ethernet, USB, and more

Quality measurements to the probe tip and jitter analysis using the DCA-J proven algorithms
A versatile instrument consisting of:
- A wide-bandwidth oscilloscope
- A digital communications analyzer
- A time-domain reflectometer
- One-button jitter analyzer

All at a cost typically less than half that of other alternatives, and compatible with every DCA plug-in customers have ever bought from Agilent.
N4903A J-BERT High-Performance Serial BERT

The high-performance Serial BERT for complete jitter tolerance testing:
- Calibrated jitter composition
- Automated jitter characterization
- Compliant to latest serial bus standards
- Integrated into one box

Covered standards include:
- PCI Express
- 10GbE/XAUI
- XFI/XFP
- FB-DIMM
- SATA II

Smartest Characterization
Manual Jitter Composition (opt-J10)

Every jitter type can be varied individually.

Various Jitter types can be combined.
Automated Jitter Tolerance Characterization (opt-J10)

Characterization of RX tolerance

Automatically search for the maximum jitter value, that the RX tolerates

Allows to set various search parameters (linear, logarithmic, binary – upwards, downwards – step sizes.....)
Automated Jitter Tolerance Compliance Test (opt-J12)

Check compliance of RX under test and determine non-compliant points.

Result is global pass/fail + list + diagram with tested points and individual pass/fail info.

for SATA, SAS, PCI-Express, XAUI, 10GbE, FB-DIMM, CEI
Total Jitter Measurements

Fast Total Jitter Measurement Measures accurately down to low BER levels

BERT Scan measurement Quickly determines TJ at low BER levels
Agilent’s Jitter solution portfolio

**Analysis**

- **Infiniium oscilloscopes and DCA-J**
  - High performance real-time scopes and wide bandwidth oscilloscope with jitter analysis

- **Serial BERTs, ParBERT**
  - Pattern generator and error detector with jitter sources and BER, jitter and eye analysis

**Generation**

- **Pulse Data Generator**
  - Leading pulse, pattern, data and clock generation for digital design

**Design Verification**

- Boards, general purpose

**Device Characterization:**

- Transceiver, MUX, SERDES, backplanes

*Agilent Technologies is the premier supplier for Physical Layer Test*
Summary

• As data rates go to 5 Gb/s and beyond, jitter measurements are more complex

• New N4903A J-BERT addresses the complexities of calibrated jitter injection and automated jitter characterization

• For additional information:
  • www.agilent.com/find/jitter
  • www.agilent.com/find/jitter_info
  • www.agilent.com/find/sigint
  • www.agilent.com/find/J-BERT
  • www.agilent.com/find/DCAJ
  • www.agilent.com/find/Infiniium

Agilent Jitter Solutions
Jitter Application Information
Other Agilent Jitter eSeminars
N4903A product page
86100C product page
DSO 80000 product page
Questions?